GT25Q16BL

16M Bits
SPI Nor Flash

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Contents

1. Features 5
2. Genera Description 6
3.Package Types: 7
3.1 Pin Configuration 7
3.2 Pin Description 8
3.3 Chip Select (/CS) 8
3.4 Serial Data Input, Output and IOs (DI, DO and IO0, IO1, IO2, IO3) 8
3.5 Write Protect (/WP) 8
3.6 HOLD (/HOLD) 8
3.7 Serial Clock (CLK) 8
4.BLOCK DIAGRAM 9
5.Memory Architecture Diagram（16Mb） 10
6. ELECTRICAL CHARACTERISTICS 11
6.1 Absolute Maximum Ratings(1) 11
6.2 Power-up Timing and Write Inhibit Threshold 11
6.3 Power Up/Down and Voltage Drop 12
6.4 DC Electrical Characteristics: Industrial: 13
6.5 DC Electrical Characteristics: Industrial: 14
6.6 AC Measurement Conditions 15
6.7 AC Characteristics 15
6.8 AC Characteristics 17
6.9 Serial Output Timing 19
6.10 Serial Input Timing 19
6.11 /HOLD Timing 19
6.12 /WP Timing 19
7 FUNCTIONAL DESCRIPTION 20
7.1 Standard SPI Instructions 20
7.2 Dual SPI Instructions 20
7.3 Quad SPI Instructions 20
7.4 QPI Instructions 20
7.5 SPI / QPI DTR Read Instructions 21
7.6 Hold Function 21
7.7 Software Reset 22
7.8 WRITE PROTECTION 22
8 STATUS REGISTERS AND INSTRUCTIONS 23
8.1 STATUS REGISTER 1 23
8.1.1 BUSY Status (BUSY) 23
8.1.2 Write Enable Latch Status (WEL) 23
8.1.3 Block Protect Bits (BP2, BP1, BP0) 23
8.1.4 Top/Bottom Block Protect (TB) 24
8.1.5 Sector/Block Protect (SEC) 24
8.1.6 Status Register Protect (SRP0) 24
8.2 STATUS REGISTER 2 25
8.2.1 Erase/Program Suspend Status (SUS) 25
8.2.2 Complement Protect (CMP) 25

8.2.3 Security Register Lock Bits (LB) 25
8.2.4 Quad Enable (QE) – Non-Volatile Writable 25
8.2.5 Lock Down and OTP (SRP1) 25
8.3 STATUS REGISTER 3 26
8.3.1 Output Driver Strength (DRV1, DRV0) – Volatile/Non-Volatile Writable 26
8.3.2 Reserved Bits – Non Functional 26
8.4 Status Register Memory Protection (CMP = 0) 27
8.5 Status Register Memory Protection (CMP = 1) 28
9 Commands DESCRIPTION 29
9.1 Commands Table 29
9.1.1 Instruction Set Table 1(Standard/Dual/Quad SPI, 3-Byte Address Mode)(1) 29
9.1.2 Instruction Set Table 2 (Dual/Quad SPI Instructions) 30
9.1.3 Instruction Set Table 5(QPI Instructions) 31
9.1.4 Instruction Set Table 7 (DTR with SPI Instructions) 32
9.1.5 Instruction Set Table 9 (DTR with QPI Instructions) 32
9.2 Manufacturer and Device Identification 33
9.3 Write Enable (WREN) (06h) 34
9.4 Write Disable (WRDI) (04h) 34
9.5 Write Enable for Volatile Status Register (50h) 35
9.6 Read Status Register (05h/35h/15h) 35
9.7 Write Status Register (WRSR) (01h/31h/11h) 37
9.8 Read Data Bytes (READ) (03h) 39
9.9 Fast Read (0Bh) 40
9.10 DTR Fast Read (0Dh) 42
9.11 Dual Output Fast Read (3Bh) 44
9.12 Quad Output Fast Read (6Bh) 45
9.13 Dual I/O Fast Read (BBH) 46
9.14 DTR Fast Read Dual I/O (BDh) 48
9.15 Quad I/O Fast Read (EBH) 50
9.16 DTR Fast Read Quad I/O (EDh) 53
9.17 Set Burst with Wrap (77H) 56
9.18 Page Program (PP) (02H) 57
9.19 Quad Page Program (32H) 59
9.20 Sector Erase (SE) (20H) 60
9.21 32KB Block Erase (BE) (52H) 61
9.22 64KB Block Erase (BE) (D8H) 62
9.23 Chip Erase (CE) (60/C7H) 63
9.24 Deep Power-Down (DP) (B9H) 64
9.25 Release from Deep Power-Down and Read Device ID (RDI) (ABH) 65
9.26 Read Manufacture Id/ Device Id (REMS) (90H) 67
9.27 Read Manufacture ID/ Device ID Dual I/O (92H) 68
9.28 Read Manufacture ID/ Device ID Quad I/O (94H) 69
9.29 Read Identification (RDID) (9FH) 70
9.30 Read Unique ID Number (4Bh) 71
9.31 Program/Erase Suspend (PES) (75H) 72
9.32 Program/Erase Resume (PER) (7AH) 74
9.33 Enable Reset (66H) and Reset (99H) 75
9.34 Read SFDP Register (5Ah) 76
9.34 Erase Security Registers (44h) 82

9.35 Program Security Registers (42h) 83
9.36 Read Security Registers (48h) 84
9.37 Set Read Parameters (C0h) 85
9.38 Burst Read with Wrap (0Ch) 86
9.39 DTR Burst Read with Wrap (0Eh) 87
9.40 Enter QPI Mode (38h) 88
9.41 Exit QPI Mode (FFh) 89
10 Package Information 90
10.1 Package SOP8 208MIL 90
10.2 Package SOP8 150MIL 91
10.3 Package TSSOP8L (173mil) 92
10.4 Package WSON8 (6*5mm) 93
10.5 Package USON8 (4*3mm) 94
10.6 Package USON8 (2*3mm) 95
10.7 Package 8Pin USON1.5*1.5 96
10.8 Package 8ball WLCSP 97
11 Ordering Information 98
12 Valid Part Numbers and Top Side Marking 99
13 REVISION HISTORY 100

1. Features

- Single Power Supply Voltage
  - Full voltage range: 1.65~3.6V
- Operating Temperature range:
  - –40 to +85 °C
  - –40 to +105 °C
- 16M-bit Serial Flash
  - 2M-byte
  - 256 bytes per programmable page
- Standard, Dual, Quad SPI
  - Standard SPI: CLK, CS#, DI, DO, WP#, HOLD#
  - Dual SPI: CLK, CS#, IO0, IO1, WP#, HOLD#
  - Quad SPI: CLK, CS#, IO0, IO1, IO2, IO3
  - SPI/QPI DTR (Double Transfer Rate) Read
  - Software & Hardware Reset
- High Speed Clock Frequency
  - 80MHz for fast read with 30PF load
  - Dual I/O Data transfer up to 160Mbits/s
  - Quad I/O Data transfer up to 320Mbits/s
- Software/Hardware Write Protection
  - Write protect all/portion of memory via software
  - Enable/Disable protection with WP# Pin
  - Top/Bottom Block protection
- Allows XIP (execute in place) Operation
  - Continuous Read With 8/16/32/64-byte Wrap
- Data Retention
  - 20-year data retention typical
- Minimum 100,000 Program/Erase Cycles
- ESD protection (Human Body Model)
  - –4000V to +4000V
- Fast Program/Erase Speed
  - Page Program time: 0.7ms typical
  - Sector Erase time: 2.5ms typical
  - Block Erase time: 2.5ms typical
  - Chip Erase time: 5ms typical
- Flexible Architecture
  - Uniform Sector of 4K-byte
  - Uniform Block of 32/64K-byte
  - Erase/Program Suspend/Resume
- Low Power Consumption
  - 7uA typical Standby current
  - 0.3uA typical power down current
- Advanced security Features
  - 4*256 Byte Security Registers With OTP Lock
  - 64-Bit Unique Serial Number for each device
- Space Efficient Packaging:
  - 8-pin SOIC 208/150 mil
  - 8-pad WSON 6X5 mm
  - 8-pad WSON 4X3 mm
  - USON8 2X3 mm
  - USON8 1.5X1.5 mm
  - 8-pin TSSOP
  - 24-ball WLCSP
  - Contact Giantec for KGD and other

2. Genera Description

GT25Q16BL is 16Mb bits Serial NOR Flash, The array is organized into 8192 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time. Pages can be erased in groups of 4 (1KB sector erase), groups of 16 (4KB Sector erase), groups of 128 (32KB block erase), groups of 256 (64KB block erase) or the entire chip (chip erase), The device operates on a single 1.65V to 3.6V power supply with current consumption as low as 1uA Standby current and 0.1μA for power-down. All devices are offered in space-saving packages.

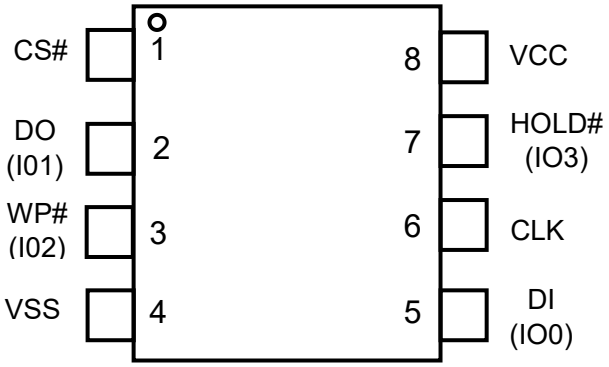
The GT25Q16BL support the standard Serial Peripheral Interface (SPI), Dual/Quad I/O SPI, Quad Peripheral Interface (QPI) as well as Double Transfer Rate (DTR): Serial Clock, Chip Select, Serial Data I/O0 (DI), I/O1 (DO), I/O2 (/WP), and I/O3 (/HOLD). SPI clock frequencies of up to 104MHz are supported allowing equivalent clock rates of 208MHz (104MHz x 2) for Dual I/O and 416MHz (104MHz x 4) for Quad I/O when using the Fast Read Dual/Quad I/O instructions. These transfer rates can outperform standard Asynchronous 8 and 16-bit Parallel Flash memories. The Continuous Read Mode allows for efficient memory access with as few as 8-clocks of instruction-overhead to read a 24-bit address, allowing true XIP (execute in place) operation.

A Hold pin, Write Protect pin and programmable write protection, with top or bottom array control, provide further control flexibility. Additionally, the device supports JEDEC standard manufacturer and device ID and SFDP Register, a 64-bit Unique Serial Number and three 1024-bytes Security Registers.

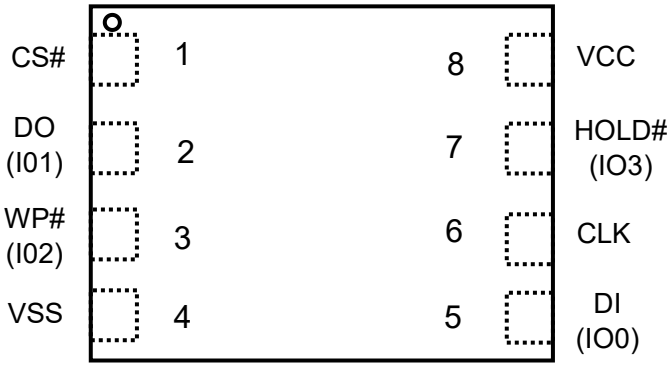
3.Package Types:

GT25Q16BL is offered in an 8-pin plastic 208mil/150-mil width SOIC (package code W/G),an 8-pad WSON 6X5-mm (package code WS) , an 8-pad WSON 4X3-mm (package code WU)，and 24-ball WLCSP as below.Package diagrams and dimensions are illustrated at the end of this datasheet.

3.1 Pin Configuration

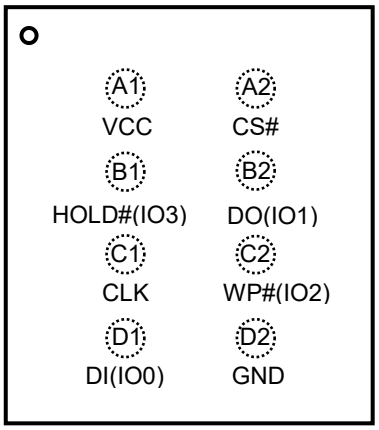


SOP8 208mil/150mil and TSSOP

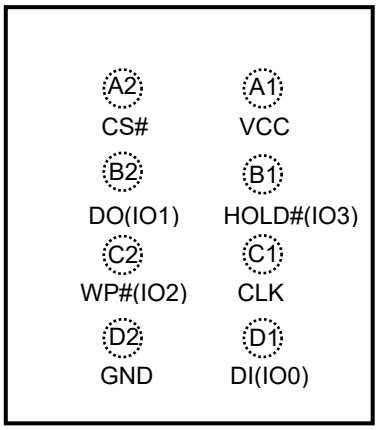


WSON 6x5/ WSON 4x3/
USON 2x3/ USON 1.5x1.5

Top View



Bottom View



8Ball WLCSP

3.2 Pin Description

Pin Name	I/O	Function
/CS	I	Chip Select Input
DO(IO1)	I/O	Data Output (Data Input Output 1)*1
/WP(I/O2)	I/O	Write Protect Input (Data Input Output 2)*2
GND		Ground
DI(I/O0)	I/O	Data Input (Data Input Output 0)*1
CLK	I	Serial Clock Input
/HOLD(I/O3)	I/O	Hold Input (Data Input Output 3)*2
VCC		Power Supply

3.3 Chip Select (/CS)

The SPI Chip Select (/CS) pin enables and disables device operation. When /CS is high the device is deselected and the Serial Data Output (DO, or IO0, IO1, IO2, IO3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress. When /CS is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device.After power-up, /CS must transition from high to low before a new instruction will be accepted. The /CS input must track the VCC supply level at power-up (see “Write Protection”). If needed a pull-up resister on /CS can be used to accomplish this.

3.4 Serial Data Input, Output and IOs (DI, DO and IO0, IO1, IO2, IO3)

The **GT25Q16BL** supports standard SPI, Dual SPI and Quad SPI operation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge of CLK.

Dual and Quad SPI instructions use the bidirectional IO pins to serially write instructions, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set.When QE=1, the /WP pin becomes IO2 and /HOLD pin becomes IO3.

3.5 Write Protect (/WP)

The Write Protect (/WP) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register’s Block Protect (CMP, SEC, TB, BP2, BP1 and BP0) bits and Status Register Protect (SRP) bits, a portion as small as a 4KB sector or the entire memory array can be hardware protected. The /WP pin is active low. When the QE bit of Status Register-2 is set for Quad I/O,the /WP pin function is not available since this pin is used for IO2.

3.6 HOLD (/HOLD)

The /HOLD pin allows the device to be paused while it is actively selected. When /HOLD is brought low,while /CS is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don’t care). When /HOLD is brought high, device operation can resume. The /HOLD function can be useful when multiple devices are sharing the same SPI signals. The /HOLD pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, the /HOLD pin function is not available since this pin is used for IO3. See the pin configuration of Quad I/O operation.

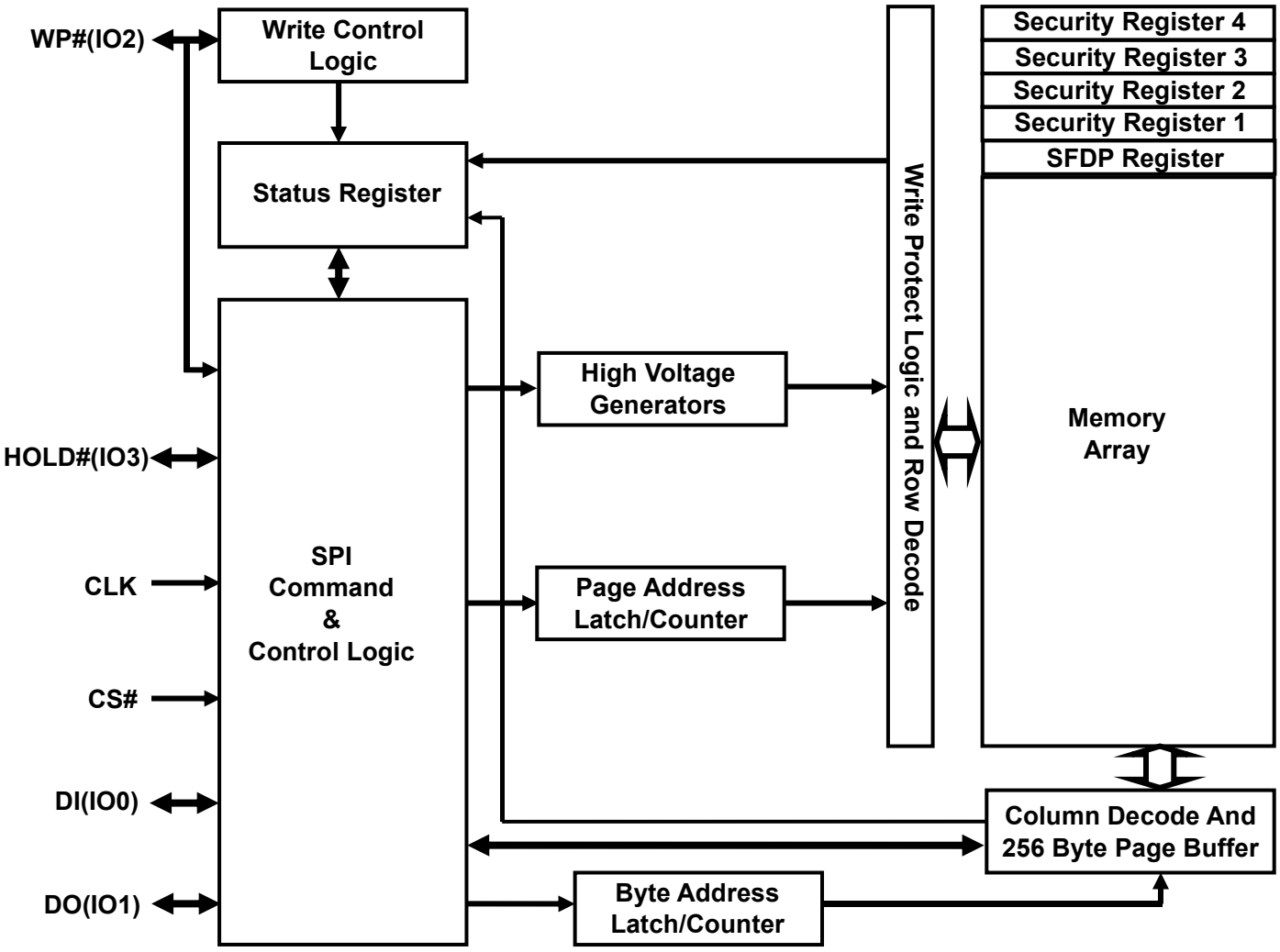
3.7 Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI Operations")

Notes:

1. IO0 and IO1 are used for Standard and Dual SPI instructions
2. IO0 – IO3 are used for Quad SPI instructions, /WP & /HOLD functions are only available for Standard/Dual SPI.

4.BLOCK DIAGRAM



5.Memory Architecture Diagram（16Mb）

64KB Block	32KB Block	4KB Block	Block Address Range	256Byte Page	Page Address Range
64KB	32KB	4KB	1FFFFFh – 1FF000h	256 Bytes	1FFFFFh – 1FFF00h
		4KB	1FEFFFh – 1FE000h	256 Bytes	1FFEFFh – 1FFE00h
		4KB	1FDFFFh – 1FD000h	256 Bytes	1FFDFFh – 1FFD00h
		4KB	1FCFFFh – 1FC000h	256 Bytes	1FFCFFh – 1FFC00h
		4KB	1FBFFFh – 1FB000h	256 Bytes	1FFBFFh – 1FFB00h
		4KB	1FAFFFh – 1FA000h	256 Bytes	1FFAFFh – 1FFA00h
		4KB	1F9FFFh – 1F9000h	256 Bytes	1FF9FFh – 1FF900h
		4KB	1F8FFFh – 1F8000h	256 Bytes	1FF8FFh – 1FF800h
	32KB	4KB	1F7FFFh – 1F7000h	256 Bytes	1FF7FFh – 1FF700h
		4KB	1F6FFFh – 1F6000h	256 Bytes	1FF6FFh – 1FF600h
		4KB	1F5FFFh – 1F5000h	256 Bytes	1FF5FFh – 1FF500h
		4KB	1F4FFFh – 1F4000h	256 Bytes	1FF4FFh – 1FF400h
		4KB	1F3FFFh – 1F3000h	256 Bytes	1FF3FFh – 1FF300h
		4KB	1F2FFFh – 1F2000h	256 Bytes	1FF2FFh – 1FF200h
		4KB	1F1FFFh – 1F1000h	256 Bytes	1FF1FFh – 1FF100h
		4KB	1F0FFFh – 1F0000h	256 Bytes	1FF0FFh – 1FF000h
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
64KB	32KB	4KB	00FFFFh – 00F000h	256 Bytes	000FFFh – 000F00h
		4KB	00EFFFh – 00E000h	256 Bytes	000EFFh – 000E00h
		4KB	00DFFFh – 00D000h	256 Bytes	000DFFh – 000D00h
		4KB	00CFFFh – 00C000h	256 Bytes	000CFFh – 000C00h
		4KB	00BFFFh – 00B000h	256 Bytes	000BFFh – 000B00h
		4KB	00AFFFh – 00A000h	256 Bytes	000AFFh – 000A00h
		4KB	009FFFh – 009000h	256 Bytes	0009FFh – 000900h
		4KB	008FFFh – 008000h	256 Bytes	0008FFh – 000800h
	32KB	4KB	007FFFh – 007000h	256 Bytes	0007FFh – 000700h
		4KB	006FFFh – 006000h	256 Bytes	0006FFh – 000600h
		4KB	005FFFh – 005000h	256 Bytes	0005FFh – 000500h
		4KB	004FFFh – 004000h	256 Bytes	0004FFh – 000400h
		4KB	003FFFh – 003000h	256 Bytes	0003FFh – 000300h
		4KB	002FFFh – 002000h	256 Bytes	0002FFh – 000200h
		4KB	001FFFh – 001000h	256 Bytes	0001FFh – 000100h
		4KB	000FFFh – 000000h	256 Bytes	0000FFh – 000000h

6. ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings(1)

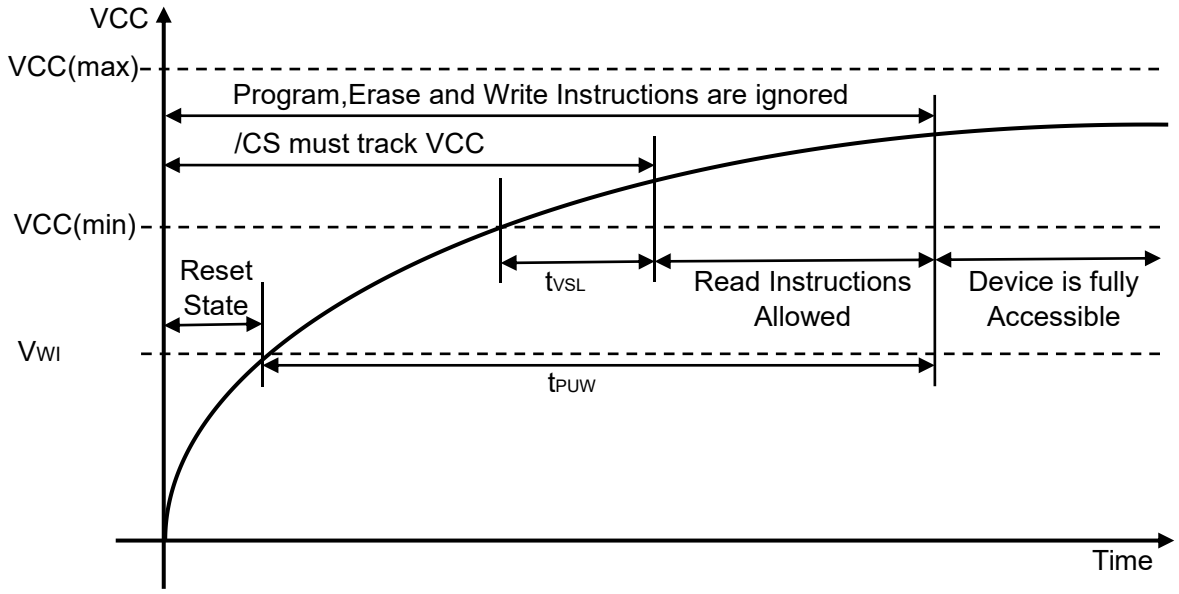
PARAMETERS	SYMBOL	CONDITIONS	RANGE	UNIT
Supply Voltage	VCC		-0.6 to VCC+0.6V	V
Voltage Applied to Any Pin	V IO	Relative to Ground	-0.6 to VCC+0.4V	V
Transient Voltage on any Pin	VIOT	<20nS Transient Relative to Ground	-2.0V to VCC+2.0V	V
Storage Temperature	TSTG		–65 to +150 °C	°C
Ambient Operating Temperature	Ta		–40 to +125 °C	°C
Electrostatic Discharge Voltage	VESD	Human Body Model(2)	–4000 to +4000 V	V

Notes:

1. This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.

2. JEDEC Std JESD22-A114A (C1=100pF, R1=1500 ohms, R2=500 ohms).

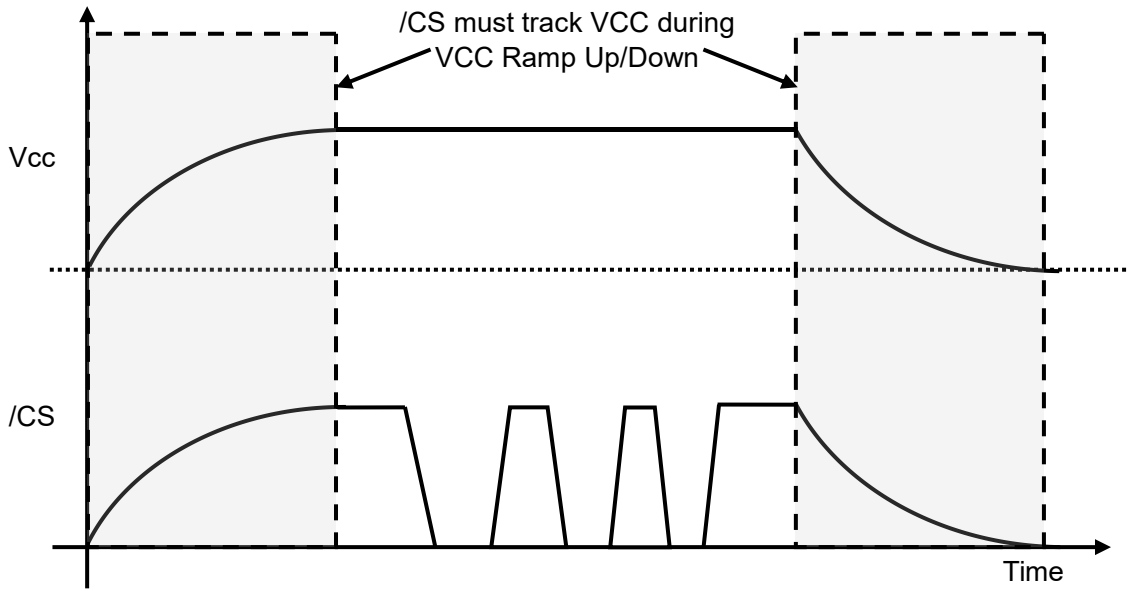
6.2 Power-up Timing and Write Inhibit Threshold

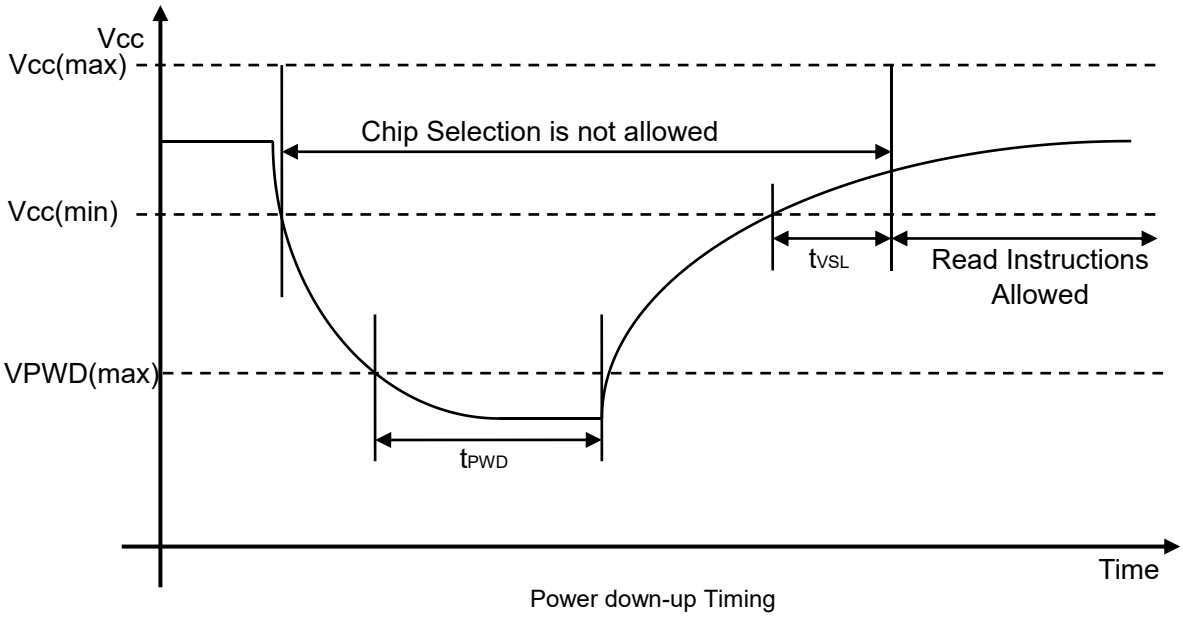


Power-up Timing and Voltage Levels

PARAMETERS	SYMBOL	spec		UNIT
		Min	Max	
VCC (min) to /CS Low	tVSL(1)	100		µs
Time Delay Before Write Instruction	tPUW(1)	5		ms
Write Inhibit Threshold Voltage	VWI(1)	1.0	1.4	V

6.3 Power Up/Down and Voltage Drop





Power down-up Timing

Symbol	Parameter	min	max	unit
V_{PWD}	VCC voltage needed to below VPWD for ensuring initialization will occur		0.5	V
t_{PWD}	The minimum duration for ensuring initialization will occur	300		us
t_{VR}	VCC Rise Time	1	500000	us/V

6.4 DC Electrical Characteristics: Industrial:

(Ta= -40℃~85℃, VCC=1.65~3.6V)

Symbol	Paraneter	Conditions	1.65 to 2.3V			2.3to 3.6V			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
ISB	Standby Current	CS#=Vcc, all other inputs at 0V or Vcc		7.0	50		7.0	50	μA
IDBD	Deep power down current	CS#=Vcc, all other inputs at 0V or Vcc		0.1	5		0.3	5	μA
ICC1	Current Read DO=Open	Fr=1MHz		0.5	3		1.5	3	mA
		Fr=33MHz		1.5	4		2.5	4	mA
		Fr=50MHz		2.0	8		3.5	8	mA
		Fr=104MHz		4.5	10		7.5	15	mA
ICC2	Program current	CS#=Vcc		0.6	3		1.5	5	mA
ICC3	Erase Current 4K	CS#=Vcc		0.5	2		1.5	5	mA
ICC4	Erase Current 32K	CS#=Vcc		0.5	2		1.5	5	mA
ICC5	Erase Current 64K	CS#=Vcc		0.5	2		1.5	5	mA
ICC6	Erase Current Chip	CS#=Vcc		0.5	2		1.5	5	mA
ILI	Input Leakage Current			0.2	0.5		0.2	0.5	μA
ILO	Output Leakage Current			0.2	0.5		0.2	0.5	μA
VIL	Input Low Voltage		-0.5		0.3VCC	-0.5		0.3VCC	V
VIH	Input High Voltage		0.7VCC		VCC+0.4	0.7VCC		VCC+0.4	V
VOL	Output Low Voltage	IOL=100μA			0.2			0.2	V
VOH	Output High Voltage	IOH=-100μA	VCC-0.2			VCC-0.2			V

Note:

1. Typical values measured at 3.0V @ 25°C for the 1.65V to 3.6V range.

6.5 DC Electrical Characteristics: Industrial:

(Ta= -40℃~105℃, VCC=1.65~3.6V)

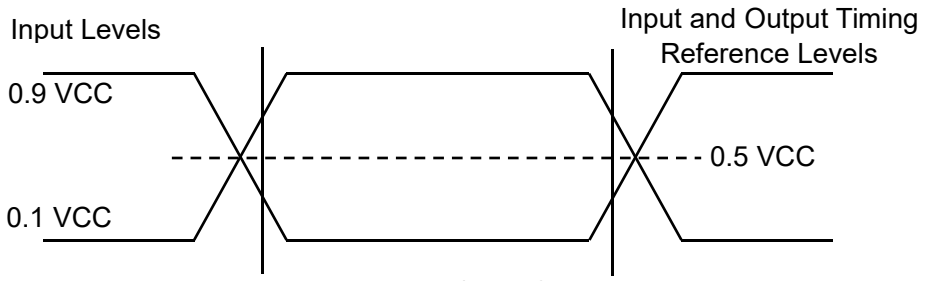
Symbol	Paraneter	Conditions	1.65 to 2.3V			2.3to 3.6V			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
ISB	Standby Current	CS#=Vcc, all other inputs at 0V or Vcc		7.0	50		7.0	50	μA
IDBD	Deep power down current	CS#=Vcc, all other inputs at 0V or Vcc		0.1	5		0.3	5	μA
ICC1	Current Read DO=Open	Fr=1MHz		0.5	3		1.5	3	mA
		Fr=33MHz		1.5	4		2.5	4	mA
		Fr=50MHz		2.0	8		3.5	8	mA
		Fr=104MHz		4.5	10		7.5	15	mA
ICC2	Program current	CS#=Vcc		0.6	3		1.5	5	mA
ICC3	Erase Current 4K	CS#=Vcc		0.5	2		1.5	5	mA
ICC4	Erase Current 32K	CS#=Vcc		0.5	2		1.5	5	mA
ICC5	Erase Current 64K	CS#=Vcc		0.5	2		1.5	5	mA
ICC6	Erase Current Chip	CS#=Vcc		0.5	2		1.5	5	mA
ILI	Input Leakage Current			0.2	0.5		0.2	0.5	μA
ILO	Output Leakage Current			0.2	0.5		0.2	0.5	μA
VIL	Input Low Voltage		-0.5		0.3VCC	-0.5		0.3VCC	V
VIH	Input High Voltage		0.7VCC		VCC+0.4	0.7VCC		VCC+0.4	V
VOL	Output Low Voltage	IOL=100μA			0.2			0.2	V
VOH	Output High Voltage	IOH=-100μA	VCC-0.2			VCC-0.2			V

Note:

1. Typical values measured at 3.0V @ 25°C for the 1.65V to 3.6V range.

6.6 AC Measurement Conditions

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
Load Capacitance	CL		30	pF
Input Rise and Fall Times	TR,TF		5	ns
Input Pulse Voltages	VIN	0.1 VCC to 0.9 VCC		V
Input Timing Reference Voltages	IN	0.3 VCC to 0.7 VCC		V
Output Timing Reference Voltages	OUT	0.5 VCC to 0.5 VCC		V



AC Measurement I/O Waveform

6.7 AC Characteristics

(Ta= -40℃~85℃, VCC=1.65~3.6V)

Symbol	Description	1.65V~3.6V			Unit
		Min.	Typ.	Max.	
Fr	Clock frequency for all instructions vdd from 2.7-3.6V except DTR&03h	D.C.		80	MHz
	Clock frequency for all instructions vdd from 2.3-2.7V except DTR&03h	D.C.		70	MHz
	Clock frequency for all instructions vdd from 1.65-2.3V except DTR&03h	D.C.		30	MHz
	Clock frequency for 03h instructions vdd from 2.3-3.6V	D.C.		50	MHz
	Clock frequency for 03h instructions vdd from 1.65-2.3V	D.C.		30	MHz
	Clock frequency for DTR instructions vdd from 2.3-3.6V	D.C.		40	MHz
	Clock frequency for DTR instructions vdd from 1.65-2.3V	D.C.		30	MHz
Tch(1)	Clock High Time	45% (1/Fc)			ns
Tcl(1)	Clock Low Time	45% (1/Fc)			ns
Tclch(4)	Clock Rise Time peak to peak	0.1			V/ns
Tchcl(4)	Clock Fall Time peak to peak	0.1			V/ns
Tslch	CS# Active Setup Time (relative to CLK)	12			ns
Tchsl	CS# Not Active Hold Time (relative to CLK)	5			ns
Tdvch	Data In Setup Time	2			ns
Tchdx	Data In Hold Time	6			ns
Tchsh	CS# Active Hold Time (relative to CLK)	5			ns

Symbol	Description	1.65V~3.6V			Unit
		Min.	Typ.	Max.	
Tshch	CS# Not Active Setup Time (relative to CLK)	20			ns
Tshsl	CS# Deselect Time From Read to next Read	20			ns
	CS# Deselect Time From Erase,Program to Read Status Register	30			ns
Tshqz(4)	Output Disable Time			50	ns
Tclqv	Clock Low to Output Valid（VCC=1.65v~2.7v）		12	17	ns
	Clock Low to Output Valid（VCC=2.7v~3.6v）		5	9	ns
Tclqx	Output Hold Time	0			ns
Thlch	HOLD# Active Setup Time (relative to CLK)	5			ns
Tchhh	HOLD# Active Hold Time (relative to CLK)	5			ns
Thhch	HOLD# Not Active Setup Time (relative to CLK)	5			ns
Tchhl	HOLD# Not Active Hold Time (relative to CLK)	5			ns
Thhqx	HOLD# to Output Low-Z			8	ns
Thlqz	HOLD# to Output High-Z			6	ns
Twhsl(3)	Write Protect Setup Time	20			ns
Tshwl(3)	Write Protect Hold Time	100			ns
Tdp	CS# High to Deep Power-down Mode			3	us
Tres1	CS# High To Standby Mode Without ID Read			20	us
Tres2	CS# High To Standby Mode With ID Read			20	us
Tsus	CS# High to next Instruction after Suspend			20	μs
Trst	CS# High to next Instruction after reset（except chip erase 60/C7h）			30	μs
	CS# High to Chip erase after reset			150	us
Tw	Write Status Register Cycle Time		3.0	5	ms
Tbp	Byte Program Time (First Byte)		100	200	μs
Tpp	Page Program Time		0.7	3	ms
Tse	Sector erase time		2.5	6	ms
Tbe1	Block erase time for 32K bytes		2.5	6	ms
Tbe2	Block erase time for 64K bytes		2.5	6	ms
Tce	Chip erase time		5	12	ms

Note:

1. tCH + tCL must be greater than or equal to 1/ Frequency.
2. Typical values given for TA=25°C. Not 100% tested.
3. Only applicable as a constraint for a WRSR instruction.
4. The value guaranteed by characterization, not 100% tested in production.

6.8 AC Characteristics

(Ta= -40℃~105℃, VCC=1.65~3.6V)

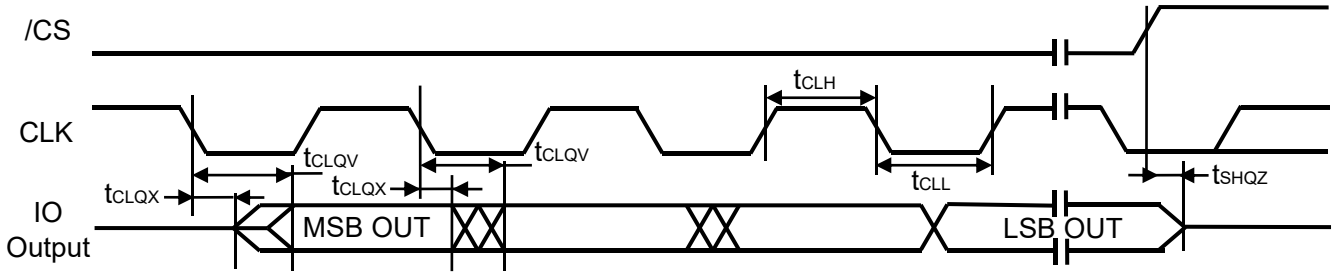
Symbol	Description	1.65V~3.6V			Unit
		Min.	Typ.	Max.	
Fr/Fc	Clock frequency for all instructions vdd from 2.7-3.6V except DTR&03h	D.C.		80	MHz
	Clock frequency for all instructions vdd from 2.3-2.7V except DTR&03h	D.C.		70	MHz
	Clock frequency for all instructions vdd from 1.65-2.3V except DTR&03h	D.C.		30	MHz
	Clock frequency for 03h instructions vdd from 2.3-3.6V	D.C.		50	MHz
	Clock frequency for 03h instructions vdd from 1.65-2.3V	D.C.		30	MHz
	Clock frequency for DTR instructions vdd from 2.3-3.6V	D.C.		40	MHz
	Clock frequency for DTR instructions vdd from 1.65-2.3V	D.C.		30	MHz
Tch(1)	Clock High Time	45% (1/Fc)			ns
Tcl(1)	Clock Low Time	45% (1/Fc)			ns
Tclch(4)	Clock Rise Time peak to peak	0.1			V/ns
Tchcl(4)	Clock Fall Time peak to peak	0.1			V/ns
Tslch	CS# Active Setup Time (relative to CLK)	12			ns
Tchsl	CS# Not Active Hold Time (relative to CLK)	5			ns
Tdvch	Data In Setup Time	2			ns
Tchdx	Data In Hold Time	6			ns
Tchsh	CS# Active Hold Time (relative to CLK)	5			ns
Tshch	CS# Not Active Setup Time (relative to CLK)	20			ns
Tshsl	CS# Deselect Time From Read to next Read	20			ns
	CS# Deselect Time From Erase,Program to Read Status Register	30			ns
Tshqz(4)	Output Disable Time			50	ns
Tclqv	Clock Low to Output Valid（VCC=1.65v~2.7v）		12	17	ns
	Clock Low to Output Valid（VCC=2.7v~3.6v）		5	9	ns
Tclqx	Output Hold Time	0			ns
Thlch	HOLD# Active Setup Time (relative to CLK)	5			ns
Tchhh	HOLD# Active Hold Time (relative to CLK)	5			ns
Thhch	HOLD# Not Active Setup Time (relative to CLK)	5			ns
Tchhl	HOLD# Not Active Hold Time (relative to CLK)	5			ns
Thhqx	HOLD# to Output Low-Z			8	ns
Thlqz	HOLD# to Output High-Z			6	ns
Twhsl(3)	Write Protect Setup Time	20			ns
Tshwl(3)	Write Protect Hold Time	100			ns
Tdp	CS# High to Deep Power-down Mode			3	us

Symbol	Description	1.65V~3.6V			Unit
		Min.	Typ.	Max.	
Tres1	CS# High To Standby Mode Without ID Read			20	us
Tres2	CS# High To Standby Mode With ID Read			20	us
Tsus	CS# High to next Instruction after Suspend			20	μs
Trst	CS# High to next Instruction after reset（except chip erase 60/C7h）			30	μs
	CS# High to Chip erase after reset			150	us
Tw	Write Status Register Cycle Time		3.0	5	ms
Tbp	Byte Program Time (First Byte)		100	200	μs
Tpp	Page Program Time		0.7	3	ms
Tse	Sector erase time		2.5	6	ms
Tbe1	Block erase time for 32K bytes		2.5	6	ms
Tbe2	Block erase time for 64K bytes		2.5	6	ms
Tce	Chip erase time		5	12	ms

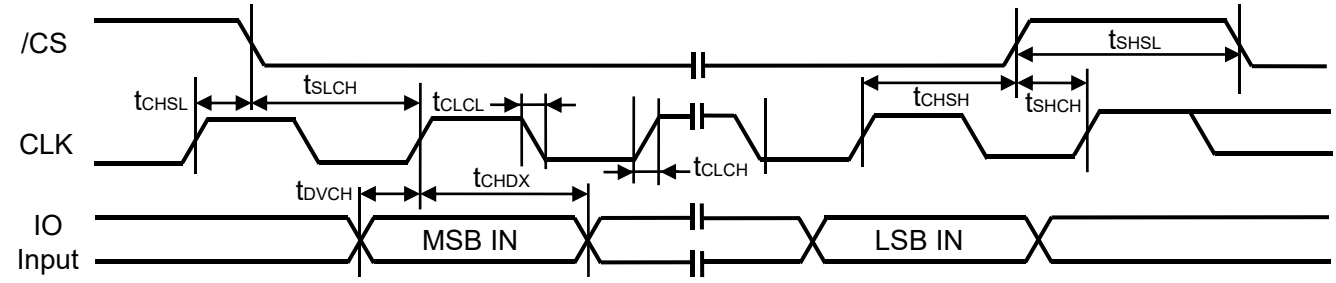
Note:

1. tCH + tCL must be greater than or equal to 1/ Frequency.
2. Typical values given for TA=25°C. Not 100% tested.
3. Only applicable as a constraint for a WRSR instruction.
4. The value guaranteed by characterization, not 100% tested in production.

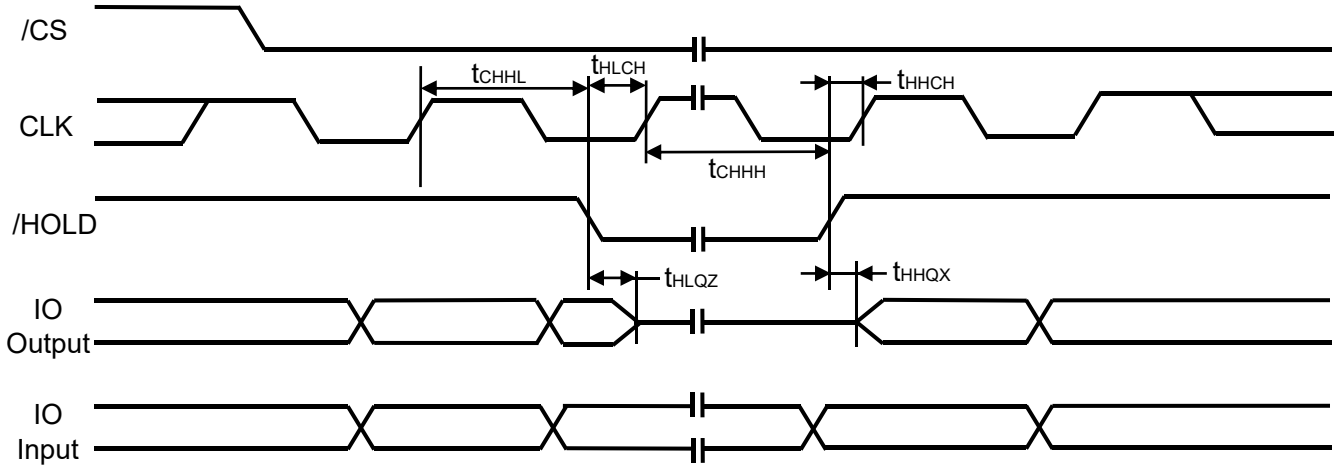
6.9 Serial Output Timing



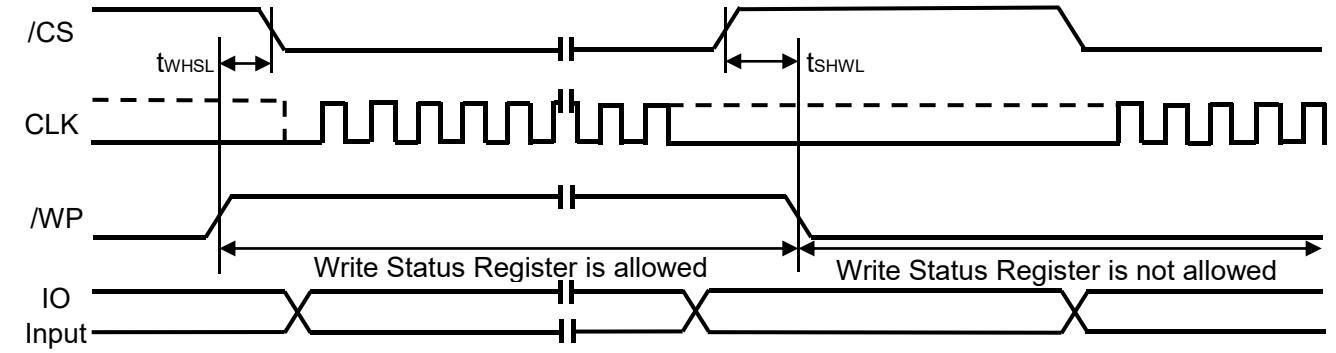
6.10 Serial Input Timing



6.11 /HOLD Timing



6.12 /WP Timing



7 FUNCTIONAL DESCRIPTION

7.1 Standard SPI Instructions

The **GT25Q16BL** is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (/CS), Serial Data Input (DI) and Serial Data Output (DO). Standard SPI instructions use the DI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The DO output pin is used to read data or status from the device on the falling edge CLK.

SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of /CS. For Mode 3, the CLK signal is normally high on the falling and rising edges of /CS.

7.2 Dual SPI Instructions

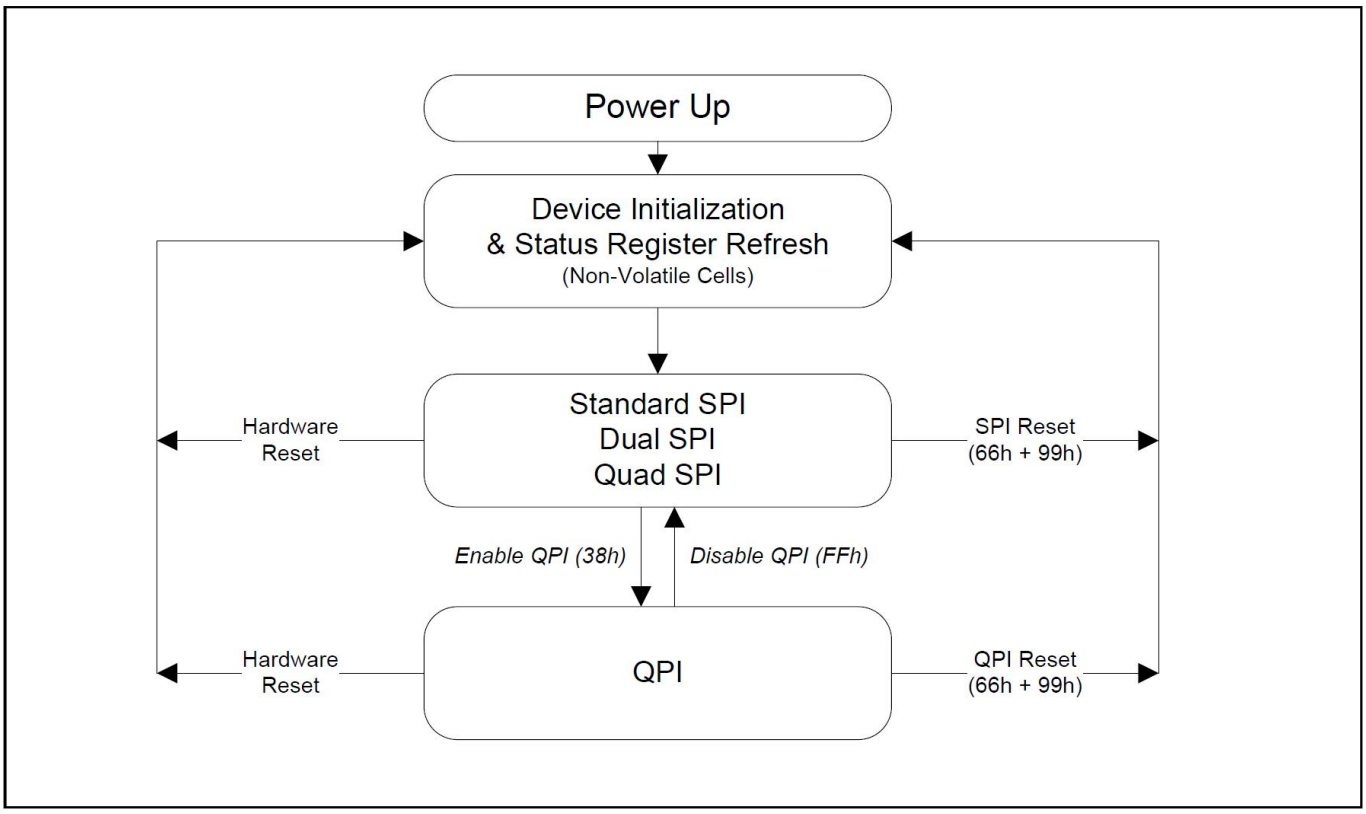
The GT25Q16BL supports Dual SPI operation when using the "Fast Read Dual Output (3Bh)" and "Fast Read Dual I/O (BBh)" instructions. These instructions allow data to be transferred to or from the device at two to three times the rate of ordinary Serial Flash devices. The Dual SPI Read instructions are ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed-critical code directly from the SPI bus (XIP). When using Dual SPI instructions, the DI and DO pins become bidirectional I/O pins: IO0 and IO1.

7.3 Quad SPI Instructions

The GT25Q16BL supports Quad SPI operation when using the "Fast Read Quad Output (6Bh)", and "Fast Read Quad I/O (EBh)" instructions. These instructions allow data to be transferred to or from the device six to eight times the rate of ordinary Serial Flash. The Quad Read instructions offer a significant improvement in continuous and random access transfer rates allowing fast code-shadowing to RAM or execution directly from the SPI bus (XIP). When using Quad SPI instructions the DI and DO pins become bidirectional IO0 and IO1, and the /WP and /HOLD pins become IO2 and IO3 respectively. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set.

7.4 QPI Instructions

The GT25Q16BL supports Quad Peripheral Interface (QPI) operations only when the device is switched from Standard/Dual/Quad SPI mode to QPI mode using the "Enter QPI (38h)" instruction. The typical SPI protocol requires that the byte-long instruction code being shifted into the device only via DI pin in eight serial clocks. The QPI mode utilizes all four IO pins to input the instruction code, thus only two serial clocks are required. This can significantly reduce the SPI instruction overhead and improve system performance in an XIP environment. Standard/Dual/Quad SPI mode and QPI mode are exclusive. Only one mode can be active at any given time. "Enter QPI (38h)" and "Exit QPI (FFh)" instructions are used to switch between these two modes. Upon power-up or after a software reset using "Reset (99h)" instruction, the default state of the device is Standard/Dual/Quad SPI mode. To enable QPI mode, the non-volatile Quad Enable bit (QE) in Status Register-2 is required to be set. When using QPI instructions, the DI and DO pins become bidirectional IO0 and IO1, and the /WP and /HOLD pins become IO2 and IO3 respectively. See Figure 3 for the device operation modes.



SPI / QPI Operations

7.5 SPI / QPI DTR Read Instructions

To effectively improve the read operation throughput without increasing the serial clock frequency,GT25Q16BL introduces multiple DTR (Double Transfer Rate) Read instructions that support Standard/Dual/Quad SPI and QPI modes. The byte-long instruction code is still latched into the device on the rising edge of the serial clock similar to all other SPI/QPI instructions. Once a DTR instruction code is accepted by the device, the address input and data output will be latched on both rising and falling edges of the serial clock.

7.6 Hold Function

For Standard SPI and Dual SPI operations, the /HOLD signal allows the GT25Q16BL operation to be paused while it is actively selected (when /CS is low). The /HOLD function may be useful in cases where the SPI data and clock signals are shared with other devices. For example, consider if the page buffer was only partially written when a priority interrupt requires use of the SPI bus. In this case the /HOLD function can save the state of the instruction and the data in the buffer so programming can resume where it left off once the bus is available again. The /HOLD function is only available for standard SPI and Dual SPI operation, not during Quad SPI. The Quad Enable Bit QE in Status Register-2 is used to determine if the pin is used as /HOLD pin or data I/O pin. When QE=0 (factory default), the pin is /HOLD, when QE=1, the pin will become an I/O pin, /HOLD function is no longer available.

To initiate a /HOLD condition, the device must be selected with /CS low. A /HOLD condition will activate on the falling edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the /HOLD condition will activate after the next falling edge of CLK. The /HOLD condition will terminate on the rising edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the /HOLD condition will terminate after the next falling edge of CLK. During a /HOLD condition, the Serial Data Output (DO) is high impedance, and Serial Data Input (DI) and Serial Clock (CLK) are ignored. The Chip Select (/CS) signal

should be kept active low for the full duration of the /HOLD operation to avoid resetting the internal logic state of the device.

7.7 Software Reset

The GT25Q16BL can be reset to the initial power-on state by a software Reset sequence in SPI mode. This sequence must include two consecutive commands: Enable Reset (66h) & Reset (99h). If the command sequence is successfully accepted, the device will take approximately 30uS (tRST) to reset. No command will be accepted during the reset period.

Note:

1. While a faster /RESET pulse (as short as a few hundred nanoseconds) will often reset the device, a 1us minimum pulse is recommended to ensure reliable operation.

7.8 WRITE PROTECTION

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern, the GT25Q16BL provides several means to protect the data from inadvertent writes.

- Device resets when VCC is below threshold
- Time delay write disable after Power-up
- Write enable/disable instructions and automatic write disable after erase or program
- Software and Hardware (/WP pin) write protection using Status Register
- Write Protection using Power-down instruction
- Lock Down write protection until next power-up
- One Time Program (OTP) write protection*

  * Note: This feature is available upon special order. Please contact Giantec for details.

Upon power-up or at power-down, the GT25Q16BL will maintain a reset condition while VCC is below the threshold value of VWI, (See Power-up Timing and Voltage Levels). While reset, all operations are disabled and no instructions are recognized. During power-up and after the VCC voltage exceeds VWI, all program and erase related instructions are further disabled for a time delay of tPUW. This includes the Write Enable, Page Program, Sector Erase, Block Erase, Chip Erase and the Write Status Register instructions. Note that the chip select pin (/CS) must track the VCC supply level at power-up until the VCC-min level and tVSL time delay is reached. If needed a pull-up resister on /CS can be used to accomplish this.

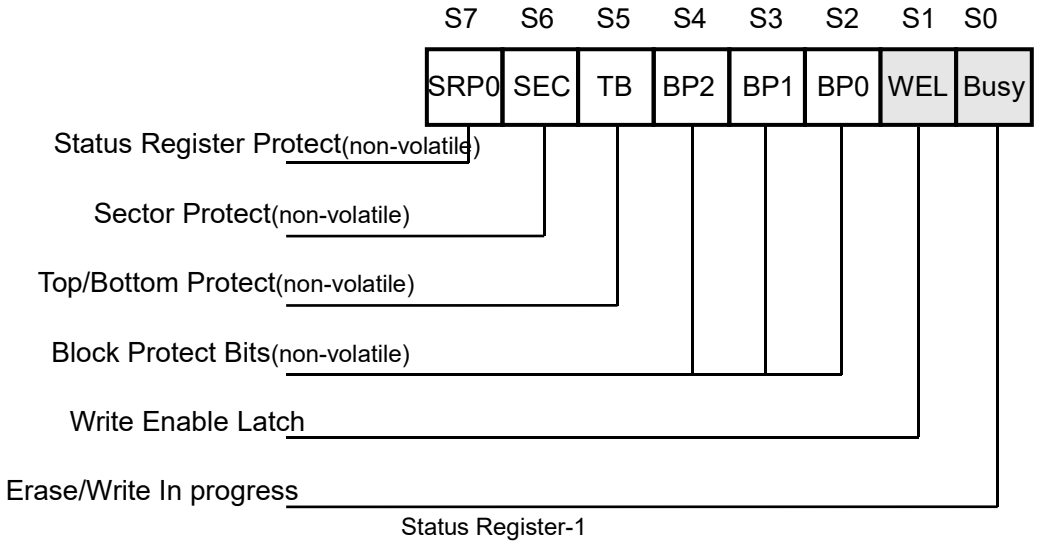
After power-up the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable instruction must be issued before a Page Program, Sector Erase, Block Erase, Chip Erase or Write Status Register instruction will be accepted. After completing a program, erase or write instruction the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register Protect (SRP, SRL) and Block Protect (CMP, SEC,TB, BP2, BP1 and BP0) bits. These settings allow a portion as small as 4KB sector or the entire memory array to be configured as read only. Used in conjunction with the Write Protect (/WP) pin, changes to the Status Register can be enabled or disabled under hardware control. See Status Register section for further information. Additionally, the Power-down instruction offers an extra level of write protection as all instructions are ignored except for the Release Power-down instruction.

8 STATUS REGISTERS AND INSTRUCTIONS

The Read Status Register-1 and Status Register-2 instructions can be used to provide status on the availability of the Flash memory array, if the device is write enabled or disabled, the state of write protection, Quad SPI setting, Security Register lock status and Erase/Program Suspend status. The Write Status Register instruction can be used to configure the device write protection features, Quad SPI setting and Security Register OTP lock. Write access to the Status Register is controlled by the state of the non-volatile Status Register Protect bits (SRP, SRL), the Write Enable instruction, and during Standard/Dual SPI operations, the /WP pin.

8.1 STATUS REGISTER 1



Status Register-1

8.1.1 BUSY Status (BUSY)

BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is executing a Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register or Erase/Program Security Register instruction. During this time the device will ignore further instructions except for the Read Status Register and Erase/Program Suspend instruction (see tW, tPP, tSE, tBE, and tCE in AC Characteristics). When the program, erase or write status/security register instruction has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further instructions.

8.1.2 Write Enable Latch Status (WEL)

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to 1 after executing a Write Enable Instruction. The WEL status bit is cleared to 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Erase Security Register and Program Security Register.

8.1.3 Block Protect Bits (BP2, BP1, BP0)

The Block Protect Bits (BP2, BP1, BP0) are non-volatile read/write bits in the status register (S4, S3, and S2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction (see tW in AC characteristics). All, none or a portion of the memory array can be protected from Program and Erase instructions (see Status Register Memory Protection table). The factory default setting for the Block Protection Bits is 0, none of the array protected.

8.1.4 Top/Bottom Block Protect (TB)

The non-volatile Top/Bottom bit (TB) controls if the Block Protect Bits (BP2, BP1, BP0) protect from the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The factory default setting is TB=0. The TB bit can be set with the Write Status Register Instruction depending on the state of the SRP and WEL bits.

8.1.5 Sector/Block Protect (SEC)

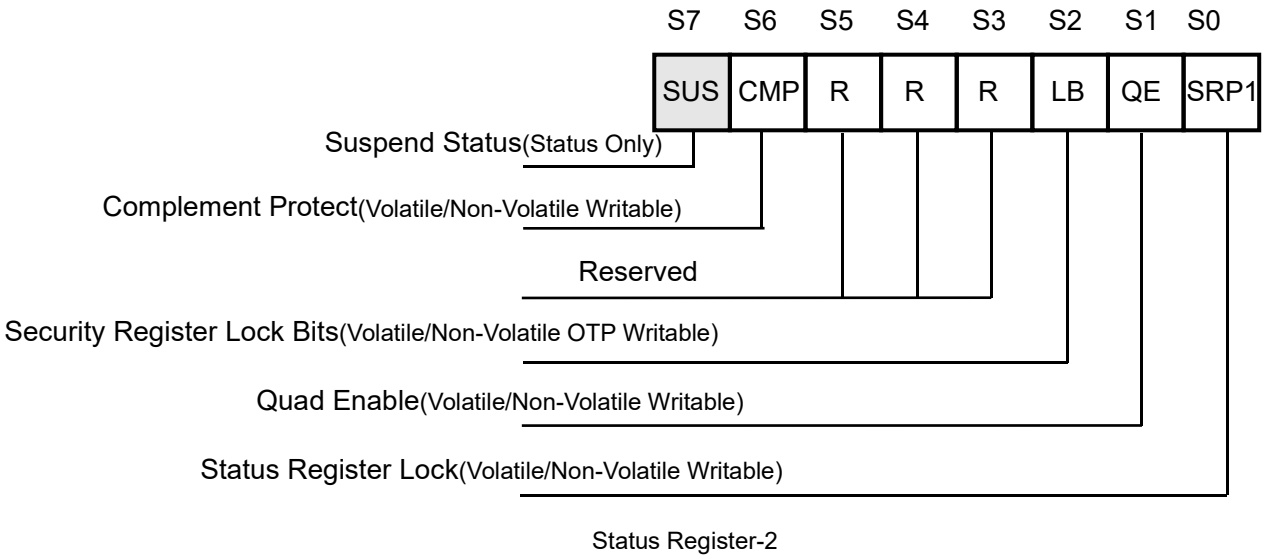
The non-volatile Sector/Block Protect bit (SEC) controls if the Block Protect Bits (BP2, BP1, BP0) protect either 4KB Sectors (SEC=1) or 64KB Blocks (SEC=0) in the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The default setting is SEC=0.

8.1.6 Status Register Protect (SRP0)

The Status Register Protect bits (SRP) are non-volatile read/write bits in the status register (S7). The SRP bits control the method of write protection: software protection.

SRP1	SRP0	/WP	Status Protection	Description
0	0	X	Software Protection	/WP pin has no control. The Status register can be written to after a Write Enable instruction, WEL=1. [Factory Default]
0	1	0	Hardware Protected	When /WP pinis low the Status Register can not be written to.
0	1	1	Hardware Unprotected	When /WP pin is high the Status register can be written to after a Write Enable instruction, WEL=1.

8.2 STATUS REGISTER 2



Status Register-2

8.2.1 Erase/Program Suspend Status (SUS)

The Suspend Status bit is a read only bit in the status register (S15) that is set to 1 after executing a Erase/Program Suspend (75H or B0H) instruction. The SUS status bit is cleared to 0 by Erase/Program Resume (7AH or 30H) instruction as well as a power-down, power-up cycle.

8.2.2 Complement Protect (CMP)

The Complement Protect bit (CMP) is a non-volatile read/write bit in the status register (S14). It is used in conjunction with SEC, TB, BP2, BP1 and BP0 bits to provide more flexibility for the array protection. Once CMP is set to 1, previous array protection set by SEC, TB, BP2, BP1 and BP0 will be reversed. For instance, when CMP=0, a top 4KB sector can be protected while the rest of the array is not; when CMP=1, the top 4KB sector will become unprotected while the rest of the array become read-only. Please refer to the Status Register Memory Protection table for details. The default setting is CMP=0.

8.2.3 Security Register Lock Bits (LB)

The Security Register Lock Bits (LB) are non-volatile One Time Program (OTP) bits in Status Register-2(S2) that provide the write protect control and status to the Security Registers. The default state of LB is 0, Security Registers are unlocked. LB can be set to 1 individually using the Write Status Register instruction. LB are One Time Programmable (OTP), once it's set to 1, the corresponding 4x256-Byte Security Register will become read-only permanently.

8.2.4 Quad Enable (QE) – Non-Volatile Writable

The Quad Enable (QE) bit is a non-volatile read/write bit in the status register (S9) that allows Quad SPI and QPI operation. When the QE bit is set to a 0 state (factory default), the /WP pin and /HOLD are enabled. When the QE bit is set to a 1, the Quad IO2 and IO3 pins are enabled, and /WP and /HOLD functions are disabled.
QE bit is required to be set to a 1 before issuing an "Enter QPI (38h)" to switch the device from Standard/Dual/Quad SPI to QPI, otherwise the command will be ignored. When the device is in QPI mode, QE bit will remain to be 1. A "Write Status Register" command in QPI mode cannot change QE bit from a "1" to a "0".

8.2.5 Lock Down and OTP (SRP1)

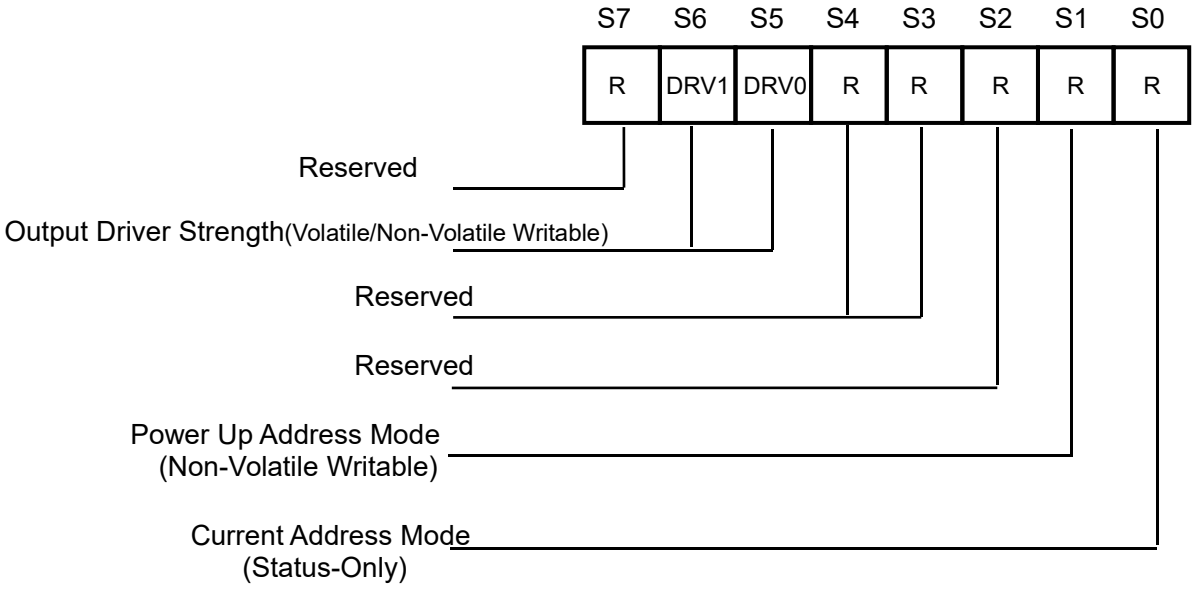
The Status Register Protect (SRP1 and SRP0) bits are non-volatile Read/Write bits in the status register. The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable protection.

SRP1	SRP0	#WP	Status Protection	Description
1	0	X	Lock-Down(1) (temporary/Volatile)	Status Register is locked by standard status register write command and can not be written to again until the next power-down, power-up cycle.
1	1	X	One Time Program(2) (Permanently/Non-Volatile)	Status Register is permanently locked by special command flow*and can not be written to

Note:

1. When SRP1=1 , a power-down, power-up cycle will change SRP1=0 state.
2. Special One Time Protection feature is available upon special order; please contact Giantec for details

8.3 STATUS REGISTER 3



Status Register-3

8.3.1 Output Driver Strength (DRV1, DRV0) – Volatile/Non-Volatile Writable

The DRV1 & DRV0 bits are used to determine the output driver strength for the Read operations.

DRV1	DRV0	Driver Strength
0	0	100%
0	1	75%
1	0	50%
1	1	25%(default)

8.3.2 Reserved Bits – Non Functional

There are a few reserved Status Register bits that may be read out as a “0” or “1”. It is recommended to ignore the values of those bits. During a “Write Status Register” instruction, the Reserved Bits can be written as “0”, but there will not be any effects.

8.4 Status Register Memory Protection (CMP = 0)

Table1

STATUS REGISTER(1)					GT25Q16BL (16M-BIT) MEMORY PROTECTION(2)			
SEC	TB	BP2	BP1	BP0	BLOCK(S)	ADDRESSES	DENSITY	PORTION
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	31	1F0000h – 1FFFFFh	64KB	Upper 1/32
0	0	0	1	0	30 and 31	1E0000h – 1FFFFFh	128KB	Upper 1/16
0	0	0	1	1	28 and 31	1C0000h – 1FFFFFh	256KB	Upper 1/8
0	0	1	0	0	24 and 31	180000h – 1FFFFFh	512KB	Upper 1/4
0	0	1	0	1	16 and 31	100000h – 1FFFFFh	1MB	Upper 1/2
0	1	0	0	1	0	000000h – 00FFFFh	64KB	Lower 1/32
0	1	0	1	0	0 and 1	000000h – 01FFFFh	128KB	Lower 1/16
0	1	0	1	1	0 thru 3	000000h – 03FFFFh	256KB	Lower 1/8
0	1	1	0	0	0 thru 7	000000h – 07FFFFh	512KB	Lower 1/4
0	1	1	0	1	0 thru 15	000000h – 0FFFFFh	1MB	Lower 1/2
X	X	1	1	X	0 thru 31	000000h – 1FFFFFh	2MB	ALL
1	0	0	0	1	31	1FF000h – 1FFFFFh	4KB	Upper 1/512
1	0	0	1	0	31	1FE000h – 1FFFFFh	8KB	Upper 1/256
1	0	0	1	1	31	1FC000h – 1FFFFFh	16KB	Upper 1/128
1	0	1	0	X	31	1F8000h – 1FFFFFh	32KB	Upper 1/64
1	1	0	0	1	0	000000h – 000FFFh	4KB	Lower 1/512
1	1	0	1	0	0	000000h – 001FFFh	8KB	Lower 1/256
1	1	0	1	1	0	000000h – 003FFFh	16KB	Lower 1/128
1	1	1	0	X	0	000000h – 007FFFh	32KB	Lower 1/64

Notes:
1. X = don’t care
2. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

8.5 Status Register Memory Protection (CMP = 1)

Table2

STATUS REGISTER(1)					GT25Q16BL (16M-BIT) MEMORY PROTECTION(2)			
SEC	TB	BP2	BP1	BP0	BLOCK(S)	ADDRESSES	DENSITY	PORTION
X	X	0	0	0	0 thru 31	000000h – 1FFFFFh	ALL	ALL
0	0	0	0	1	0 thru 30	000000h – 1EFFFFh	1984KB	Lower 31/32
0	0	0	1	0	0 thru 29	000000h – 1DFFFFh	1920KB	Lower 15/16
0	0	0	1	1	0 thru 27	000000h – 1BFFFFh	1792KB	Lower 7/8
0	0	1	0	0	0 thru 23	000000h – 17FFFFh	1536KB	Lower 3/4
0	0	1	0	1	0 thru 15	000000h – 0FFFFFh	1MB	Lower 1/2
0	1	0	0	1	1 thru 31	010000h – 1FFFFFh	1984KB	Upper 31/32
0	1	0	1	0	2 thru 31	020000h – 1FFFFFh	1920KB	Upper 15/16
0	1	0	1	1	4 thru 31	040000h – 1FFFFFh	1792KB	Upper 7/8
0	1	1	0	0	8 thru 31	080000h – 1FFFFFh	1536KB	Upper 3/4
0	1	1	0	1	16 thru 31	100000h – 1FFFFFh	1MB	Upper 1/2
X	X	1	1	X	NONE	NONE	NONE	NONE
1	0	0	0	1	0 thru 31	000000h – 1FEFFFh	2044KB	Lower 511/512
1	0	0	1	0	0 thru 31	000000h – 1FDFFFh	2040KB	Lower 255/256
1	0	0	1	1	0 thru 31	000000h – 1FBFFFh	2032KB	Lower 127/128
1	0	1	0	X	0 thru 31	000000h – 1F7FFFh	2016KB	Lower 63/64
1	1	0	0	1	0 thru 31	001000h – 1FFFFFh	2044KB	Upper 511/512
1	1	0	1	0	0 thru 31	002000h – 1FFFFFh	2040KB	Upper 255/256
1	1	0	1	1	0 thru 31	004000h – 1FFFFFh	2032KB	Upper 127/128
1	1	1	0	X	0 thru 31	008000h – 1FFFFFh	2016KB	Upper 63/64

Notes:

1. X = don't care
2. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

9 Commands DESCRIPTION

The Standard/Dual/Quad SPI instruction set of the GT25Q16BL consists of 48 basic instructions that are fully controlled through the SPI bus (see Instruction Set Table1-2). Instructions are initiated with the falling edge of Chip Select (/CS). The first byte of data clocked into the DI input provides the instruction code. Data on the DI input is sampled on the rising edge of clock with most significant bit (MSB) first.

The QPI instruction set of the GT25Q16BL consists of 35 basic instructions that are fully controlled through the SPI bus (see Instruction Set Table 3). Instructions are initiated with the falling edge of Chip Select (/CS). The first byte of data clocked through IO[3:0] pins provides the instruction code. Data on all four IO pins are sampled on the rising edge of clock with most significant bit (MSB) first. All QPI instructions, addresses, data and dummy bytes are using all four IO pins to transfer every byte of data with every two serial clocks (CLK).

Instructions vary in length from a single byte to several bytes and may be followed by address bytes, data bytes, dummy bytes (don't care), and in some cases, a combination. Instructions are completed with the rising edge of edge /CS. Clock relative timing diagrams for each instruction are included in Figures 5 through 57. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte boundary (/CS driven high after a full 8-bits have been clocked) otherwise the instruction will be ignored. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, or when the Status Register is being written, all instructions except for Read Status Register will be ignored until the program or erase cycle has completed.

9.1 Commands Table

9.1.1 Instruction Set Table 1(Standard/Dual/Quad SPI, 3-Byte Address Mode)(1)

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte6	Byte 7
Write Enable	06h						
Volatile SR Write Enable	50h						
Write Disable	04h						
Release Power-down / ID	ABh	Dummy	Dummy	Dummy	(ID7-ID0)(2)		
Manufacturer/Device ID	90h	Dummy	Dummy	00h	(MF7-MF0)	(ID7-ID0)	
JEDEC ID	9Fh	(MF7-MF0)	(ID15-ID8)	(ID7-ID0)			
Read Unique ID	4Bh	Dummy	Dummy	Dummy	Dummy	(UID63-0)	
Read Data	03h	A23-A16	A15-A8	A7-A0	(D7-D0)		
Fast Read	0Bh	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	
Page Program	02h	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0(3)	continuous
Sector Erase (4KB)	20h	A23-A16	A15-A8	A7-A0			
Block Erase (32KB)	52h	A23-A16	A15-A8	A7-A0			
Block Erase (64KB)	D8h	A23-A16	A15-A8	A7-A0			
Chip Erase	C7h/60h						
Read Status Register-1	05h	(S7-S0)(2)					
Write Status Register-1(4)	01h	(S7-S0)(4)					
Read Status Register-2	35h	(S15-S8)(2)					
Write Status Register-2	31h	(S15-S8)					

Command Name	Byte 1	Byte 2	Byte 3	c	Byte 5	Byte6	Byte7
Read Status Register-3	15h	(S23-S16)(2)					
Write Status Register-3	11h	(S23-S16)					
Read SFDP Register	5Ah	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	
Erase Security Register(5)	44h	A23-A16	A15-A8	A7-A0	(ID7-ID0)		
Program Security Register(5)	42h	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0(3)	
Read Security Register(5)	48h	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	
Erase / Program Suspend	75h						
Erase / Program Resume	7Ah						
Power-down	B9h						
Enter QPI Mode	38h						
Enable Reset	66h						
Reset Device	99h						

9.1.2 Instruction Set Table 2 (Dual/Quad SPI Instructions)

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte6	Byte 7	Byte 8	Byte 9
Fast Read Dual Output	3Bh	A23-A16	A15-A8	A7-A0	Dummy	Dummy	(D7-D0)(7)	…	
Mftr./Device ID Dual I/O	92h	A23-A16	A15-A8	00	Dummy(14)	(MF7-MF0)	(ID7-ID0)		
Fast Read Dual I/O	BBh	A23-A16	A15-A8	A7-A0	M7-M0	(D7-D0)	…		
Quad Input Page Program	32h	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0	…	…	
Fast Read Quad Output	6Bh	A23-A16	A15-A8	A7-A0	Dummy	Dummy	Dummy	Dummy	(D7-D0)(9)
Mftr./Device ID Quad I/O	94h	A23-A16	A15-A8	0	Dummy(14)	Dummy	Dummy	MF7-MF0	(ID7-ID0)
Fast Read Quad I/O	EBh	A23-A16	A15-A8	A7-A0	MF7-MF0	Dummy	Dummy	(D7-D0)	…
Set Burst with Wrap	77h	Dummy	Dummy	Dummy	W7-W0				

9.1.3 Instruction Set Table 5(QPI Instructions)

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte6	Byte 7
Write Enable	06h						
Volatile SR Write Enable	50h						
Write Disable	04h						
Release Power-down / ID	ABh	Dummy	Dummy	Dummy	(ID7-ID0)(2)		
Manufacturer/Device ID	90h	Dummy	Dummy	00h	(MF7-MF0)	(ID7-ID0)	
JEDEC ID	9Fh	(MF7-MF0)	(ID15-ID8)	(ID7-ID0)			
Set Read Parameters C0h P7-P0	C0h	P7-P0					
Fast Read	0Bh	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	
Burst Read with Wrap	0Ch	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	
Fast Read Quad I/O	EBh	A23-A16	A15-A8	A7-A0	M7-M0	(D7-D0)	
Page Program	02h	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0(3)	
Sector Erase (4KB)	20h	A23-A16	A15-A8	A7-A0			
Block Erase (32KB)	52h	A23-A16	A15-A8	A7-A0			
Block Erase (64KB)	D8h	A23-A16	A15-A8	A7-A0			
Chip Erase	C7h/60h						
Read Status Register-1	05h	(S7-S0)(2)					
Write Status Register-1(4)	01h	(S7-S0)(4)					
Read Status Register-2	35h	(S15-S8)(2)					
Write Status Register-2	31h	(S15-S8)					
Read Status Register-3	15h	(S23-S16)(2)					
Write Status Register-3	11h	(S23-S16)					
Erase / Program Suspend	75h						
Erase / Program Resume	7Ah						
Power-down	B9h						
Enable Reset	66h						
Reset Device	99h						
Exit QPI Mode	FFh						

9.1.4 Instruction Set Table 7 (DTR with SPI Instructions)

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte6	Byte 7
DTR Fast Read	0Dh	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	
DTR Fast Read Dual I/O	BDh	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	(D7-D0)
DTR Fast Read Quad I/O	EDh	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	(D7-D0)

9.1.5 Instruction Set Table 9 (DTR with QPI Instructions)

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte6	Byte 7
DTR Read with Wrap	0Dh	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	
DTR Fast Read	0Eh	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	
DTR Fast Read	EDh	A23-A16	A15-A8	A7-A0	M7-M0	(D7-D0)	

NOTE:

1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis "( )" indicate data output from the device on either 1, 2 or 4 IO pins.
2. The Status Register contents and Device ID will repeat continuously until /CS terminates the instruction.
3. At least one byte of data input is required for Page Program, Quad Page Program and Program Security Registers, up to 256 bytes of data input. If more than 256 bytes of data are sent to the device, the addressing will wrap to the beginning of the page and overwrite previously sent data.
4. Write Status Register-1 (01h) can also be used to program Status Register-1&2, see section 8.2.5.
5. Security Register Address:
   Security Register 1: A23-16 = 00h; A15-8 = 00h; A7-0 = byte address
   Security Register 2: A23-16 = 00h; A15-8 = 01h; A7-0 = byte address
   Security Register 3: A23-16 = 00h; A15-8 = 02h; A7-0 = byte address
   Security Register 3: A23-16 = 00h; A15-8 = 03h; A7-0 = byte address
6. Dual SPI address input format:
   IO0 = A22, A20, A18, A16, A14, A12, A10, A8 A6, A4, A2, A0, M6, M4, M2, M0
   IO1 = A23, A21, A19, A17, A15, A13, A11, A9 A7, A5, A3, A1, M7, M5, M3, M1
7. Dual Output data
   IO0 = (D6, D4, D2, D0)
   IO1 = (D7, D5, D3, D1)
8. Quad SPI address input format:
   IO0 = A20, A16, A12, A8, A4, A0, M4, M0
   IO1 = A21, A17, A13, A9, A5, A1, M5, M1
   IO2 = A22, A18, A14, A10, A6, A2, M6, M2
   IO3 = A23, A19, A15, A11, A7, A3, M7, M3

   Set Burst with Wrap input format:
   IO0 = x, x, x, x, x, x, W4, x
   IO1 = x, x, x, x, x, x, W5, x
   IO2 = x, x, x, x, x, x, W6, x
   IO3 = x, x, x, x, x, x, x, x
9. Quad Output Data
   IO0 = (D4, D0, ...)
   IO1 = (D5, D1, ...)
   IO2 = (D6, D2, ...)
   IO3 = (D7, D3,.....)
10. Fast Read Quad I/O Data
   IO0 = (x, x, x, x, D4, D0, D4, D0)
   IO1 =(x, x, x, x, D5, D1, D5, D1)
   IO2 =(x, x, x, x, D6, D2, D6, D2)
   IO3 =(x, x, x, x, D7, D3, D7, D3)

11. QPI Command, Address, Data input/output format:

CLK	#	0	1	2	3	4	5	6	7	8	9	10	11
IO0	=	C4	C0	A20	A16	A12	A8	A4	A0	D4	D0	D4	D0
IO1	=	C5	C1	A21	A17	A13	A9	A5	A1	D5	D1	D5	D1
IO2	=	C6	C2	A22	A18	A14	A10	A6	A2	D6	D2	D6	D2
IO3	=	C7	C3	A23	A19	A15	A11	A7	A3	D7	D3	D7	D3

12. The number of dummy clocks for QPI Fast Read, QPI Fast Read Quad I/O & QPI Burst Read with Wrap is controlled by read parameter P7 – P4.
13. The wrap around length for QPI Burst Read with Wrap is controlled by read parameter P3 – P0.

14. The first dummy is M7-M0 should be set to Fxh; if not use Read Command Bypass Mode.

9.2 Manufacturer and Device Identification

Command	M7-M0	ID15-ID8	ID7-ID0
9FH	C4h	60	15
90H	C4h		14
ABH			14

9.3 Write Enable (WREN) (06h)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE), Write Status Register (WRSR) and Erase/Program Security Registers command. The Write Enable (WREN) command sequence: CS# goes low →sending the Write Enable command → CS# goes high.

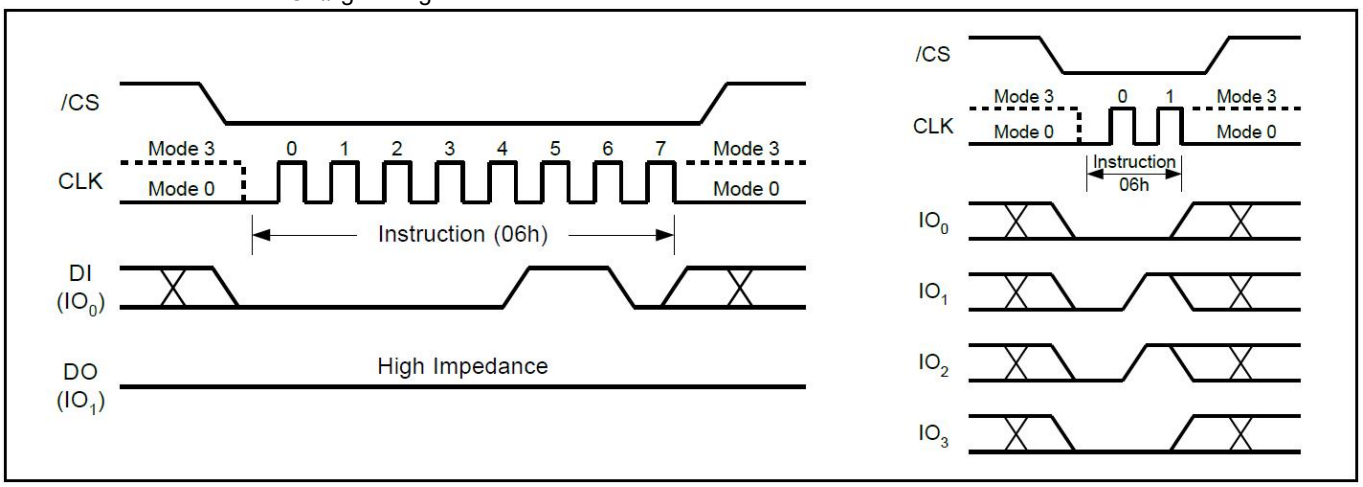


Figure1 Write Enable Sequence Diagram for SPI mode(left) or QPI Mode(Right)

9.4 Write Disable (WRDI) (04h)

The Write Disable command is for resetting the Write Enable Latch (WEL) bit. The Write Disable command sequence: CS# goes low →Sending the Write Disable command →CS# goes high. The WEL bit is reset by following condition: Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase, Chip Erase, Erase/Program Security Registers and Reset commands.

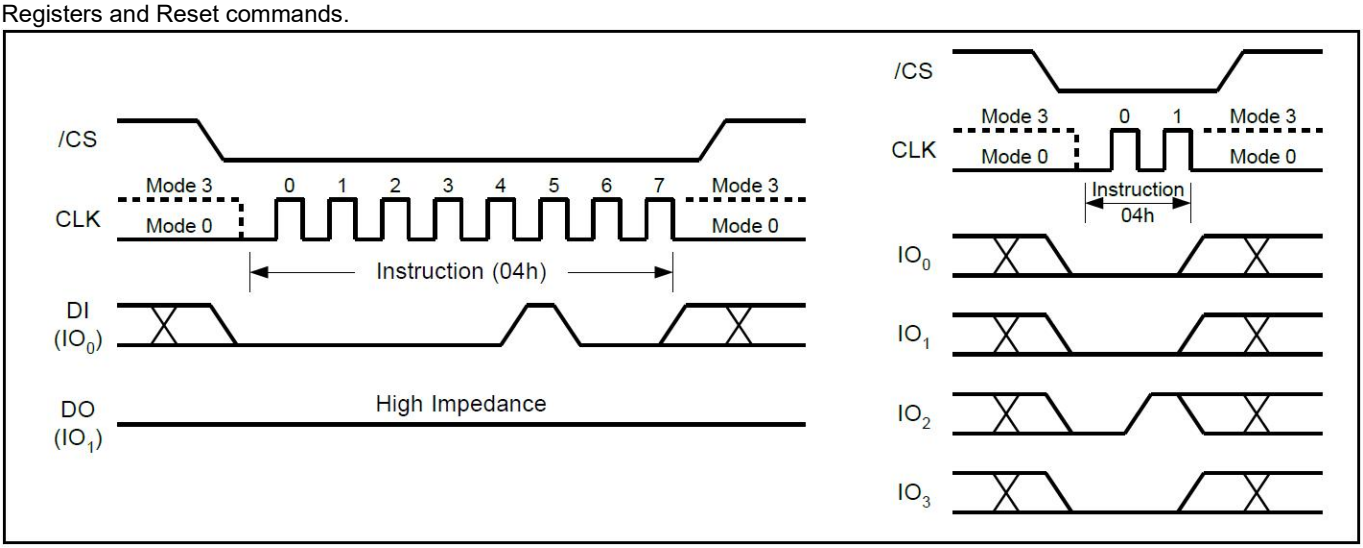


Figure2. Write Disable Sequence Diagram for SPI mode(left) or QPI Mode(Right)

9.5 Write Enable for Volatile Status Register (50h)

The non-volatile Status Register bits can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits.The Write Enable for Volatile Status Register command must be issued prior to a Write Status Register command and any other commands can't be inserted between them. Otherwise, Write Enable for Volatile Status Register will be cleared. The Write Enable for Volatile Status Register command will not set the Write Enable Latch bit, it is only valid for the Write Status Register command to change the volatile Status Register bit values.

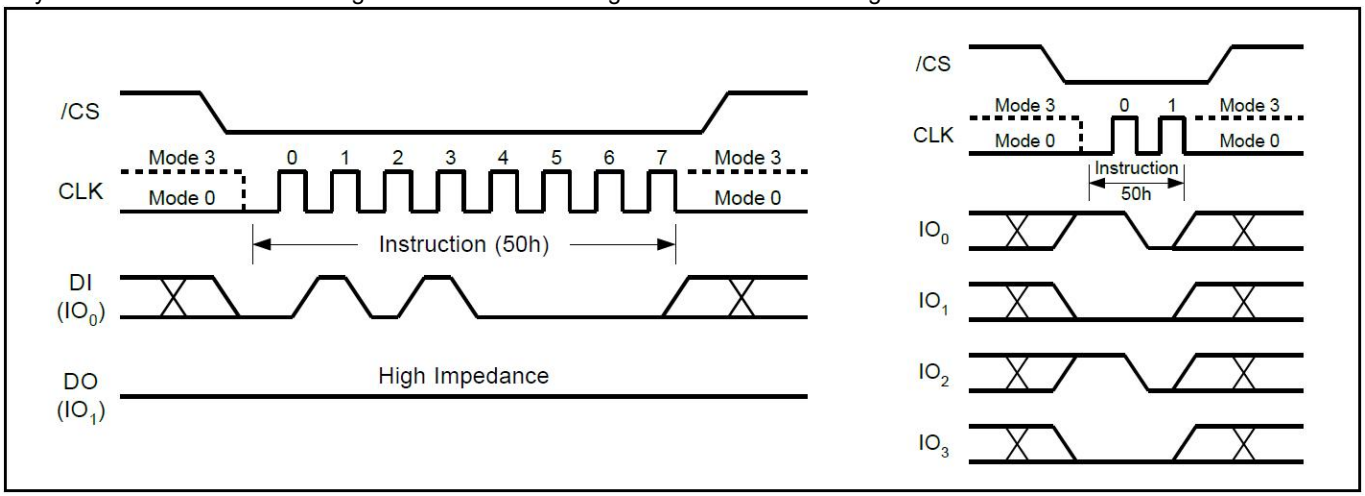


Figure3. Write Enable for Volatile Status Register Sequence Diagram for SPI mode(left) or QPI Mode(Right)

9.6 Read Status Register (05h/35h/15h)

The Read Status Register instructions allow the 8-bit Status Registers to be read. The instruction is entered by driving /CS low and shifting the instruction code "05h" for Status Register-1 or "35h" for Status Register-2 or "15h" for Status Register-3 into the DI pin on the rising edge of CLK. The status register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in figure 4. The Status Register bits are shown in Status register1 and 2 include the BUSY, WEL, BP2-BP0, TB, SEC, SRP, SRL, QE, LB[3:0], CMP and SUS bits (see Status Register section earlier in this datasheet).

The Read Status Register instruction may be used at any time, even while a Program, Erase or Write Status Register cycle is in progress. This allows the BUSY status bit to be checked to determine when the cycle is complete and if the device can accept another instruction. The Status Register can be read continuously, as shown in Figure 4. The instruction is completed by driving /CS high.

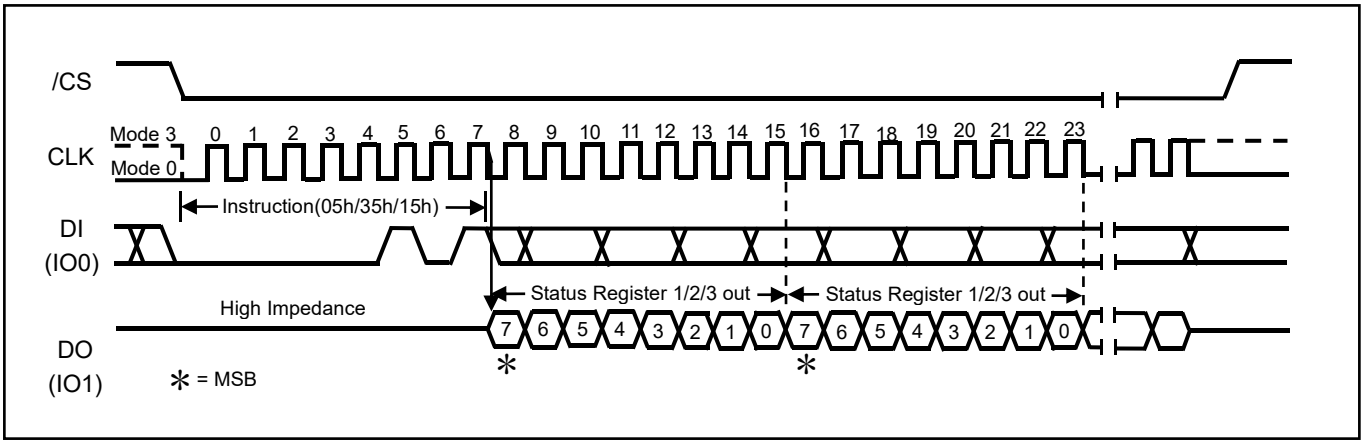


Figure4a. Read Status Register Sequence Diagram for SPI mode

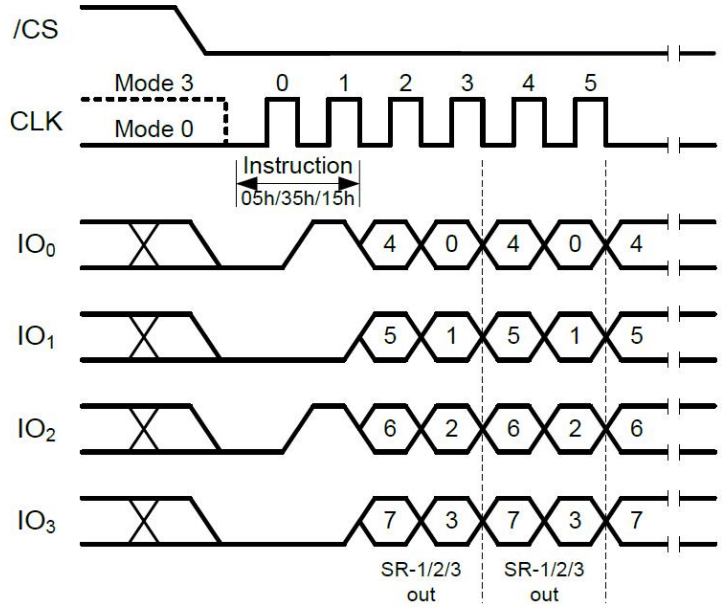


Figure4b. Read Status Register Sequence Diagram for QPI Mode

9.7 Write Status Register (WRSR) (01h/31h/11h)

The Write Status Register instruction allows the Status Registers to be written. The writable Status Register bits include: SRP, SEC, TB, BP[2:0] in Status Register-1; CMP, LB, QE, SRL in Status Register-2;DRV1, DRV0 in Status Register-3. All other Status Register bit locations are read-only and will not be affected by the Write Status Register instruction. LB are non-volatile OTP bits, once it is set to 1, it cannot be cleared to 0.

To write non-volatile Status Register bits, a standard Write Enable (06h) instruction must previously have been executed for the device to accept the Write Status Register instruction (Status Register bit WEL must equal 1). Once write enabled, the instruction is entered by driving /CS low, sending the instruction code “01h/31h/11h”, and then writing the status register data byte as illustrated in Figure 5a & 5b.

To write volatile Status Register bits, a Write Enable for Volatile Status Register (50h) instruction must have been executed prior to the Write Status Register instruction (Status Register bit WEL remains 0). However, SRL and LB cannot be changed from “1” to “0” because of the OTP protection for these bits. Upon power off or the execution of a Software/Hardware Reset, the volatile Status Register bit values will be lost, and the non-volatile Status Register bit values will be restored.

During non-volatile Status Register write operation (06h combined with 01h/31h/11h), after /CS is driven high, the self-timed Write Status Register cycle will commence for a time duration of tW (See AC Characteristics). While the Write Status Register cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Write Status Register cycle and a 0 when the cycle is finished and ready to accept other instructions again. After the Write Status Register cycle has finished, the Write Enable Latch (WEL) bit in the Status Register will be cleared to 0.

During volatile Status Register write operation (50h combined with 01h/31h/11h), after /CS is driven high, the Status Register bits will be refreshed to the new values within the time period of tSHSL2 (See AC Characteristics). BUSY bit will remain 0 during the Status Register bit refresh period.

The Write Status Register instruction can be used in both SPI mode and QPI mode. However, the QE bit cannot be written to when the device is in the QPI mode, because QE=1 is required for the device to enter and operate in the QPI mode.

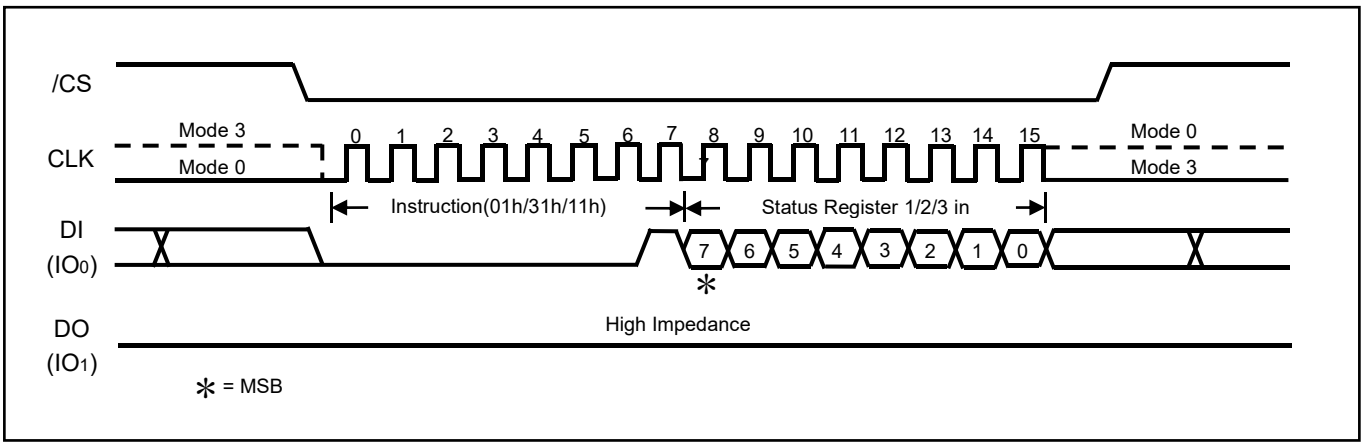


Figure5a. Write Status Register Sequence Diagram for SPI Mode

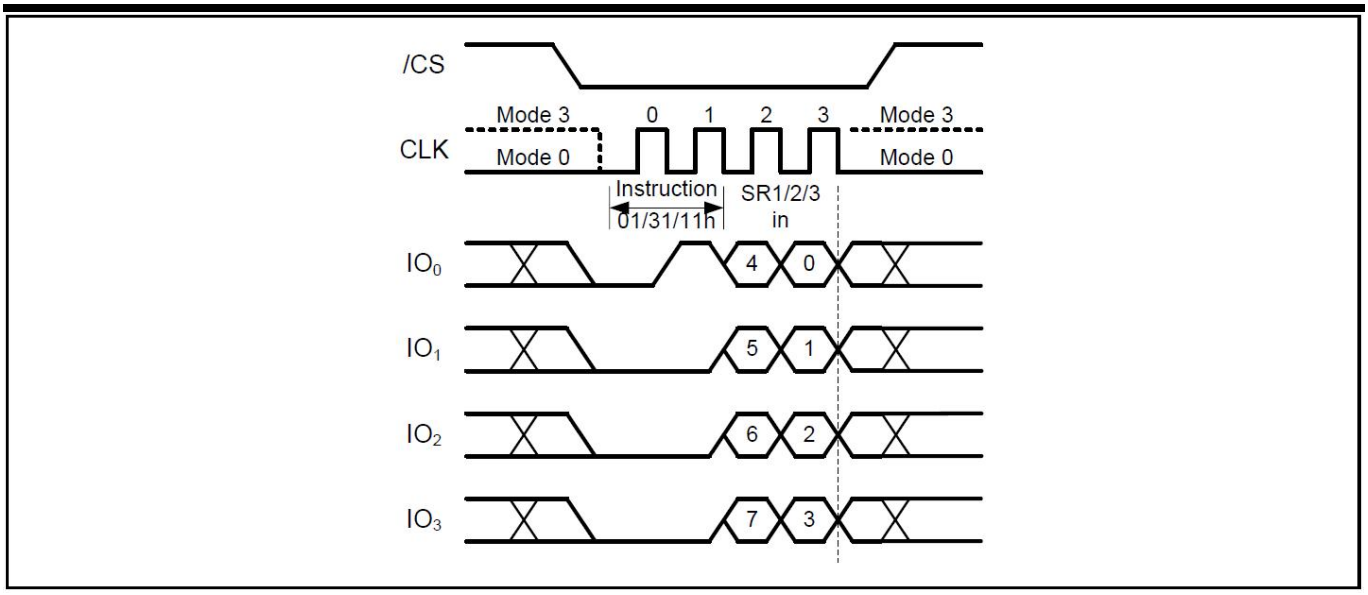


Figure5b. Write Status Register Sequence Diagram for QPI mode

The GT25Q16BL is also backward compatible to Giantec's previous generations of serial flash memories, in which the Status Register-1&2 can be written using a single "Write Status Register-1 (01h)" command. To complete the Write Status Register-1&2 instruction, the /CS pin must be driven high after the sixteenth bit of data that is clocked in as shown in Figure 9c & 9d. If /CS is driven high after the eighth clock, the Write Status Register-1 (01h) instruction will only program the Status Register-1, the Status Register-2 will not be affected (Previous generations will clear CMP and QE bits).

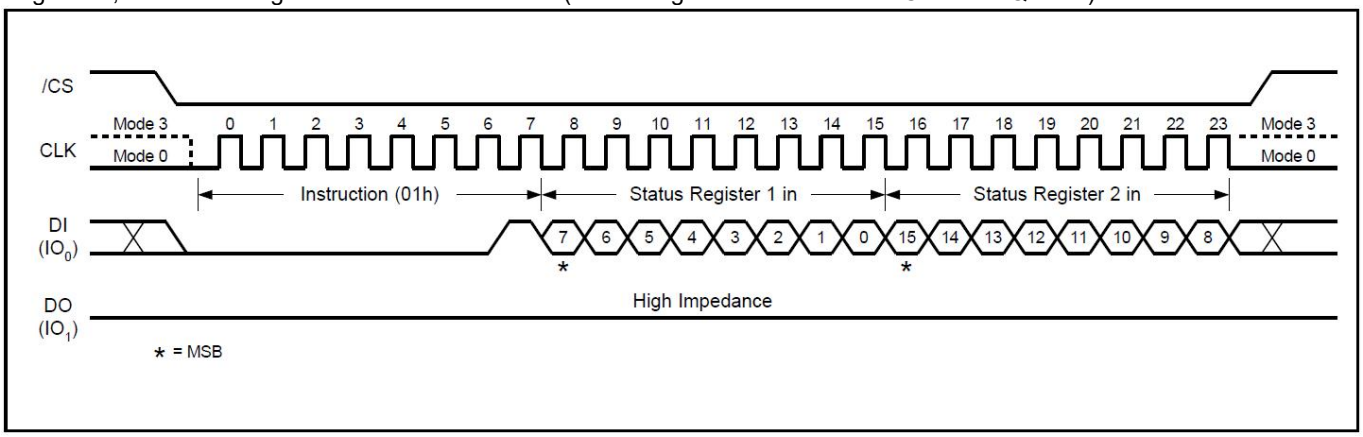


Figure5c. Write Status Register Sequence Diagram

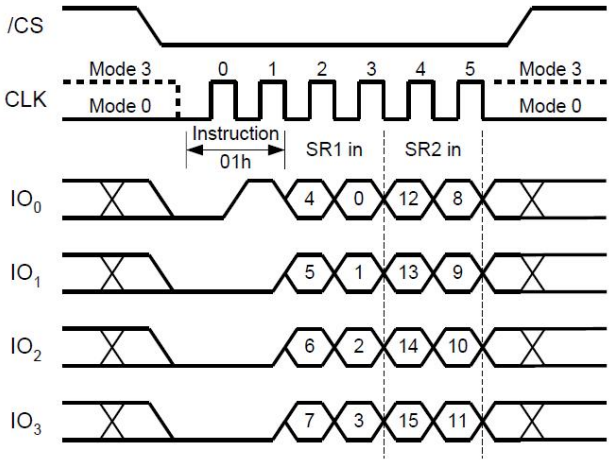


Figure5d. Write Status Register Sequence Diagram

9.8 Read Data Bytes (READ) (03h)

The Read Data instruction allows one or more data bytes to be sequentially read from the memory. The instruction is initiated by driving the /CS pin low and then shifting the instruction code “03h” followed by a 24-bit address (A23-A0) into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues. The instruction is completed by driving /CS high.

The Read Data instruction sequence is shown in Figure 6. If a Read Data instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle. The Read Data instruction allows clock rates from D.C. to a maximum of fR (see AC Electrical Characteristics).

The Read Data (03h) instruction is only supported in Standard SPI mode.

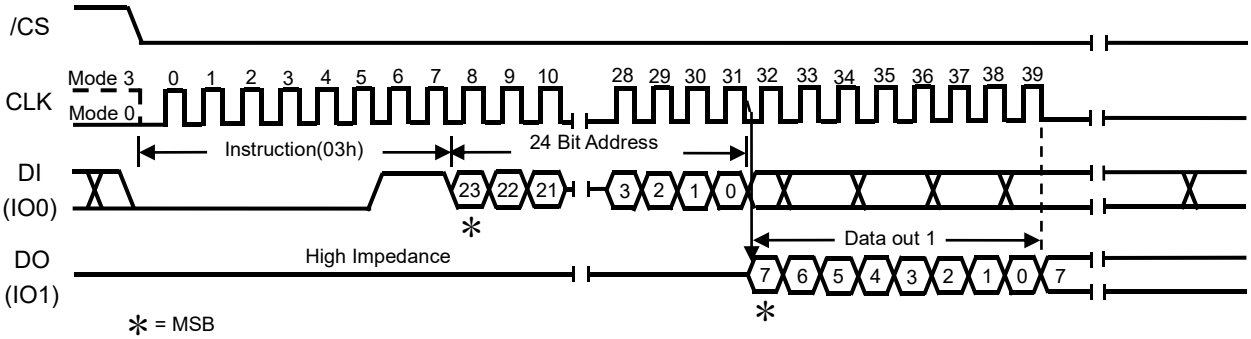


Figure 6. Read Data Bytes Sequence Diagram

9.9 Fast Read (0Bh)

The Fast Read instruction is similar to the Read Data instruction except that it can operate at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in Figure 7a. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the DO pin is a “don’t care”.

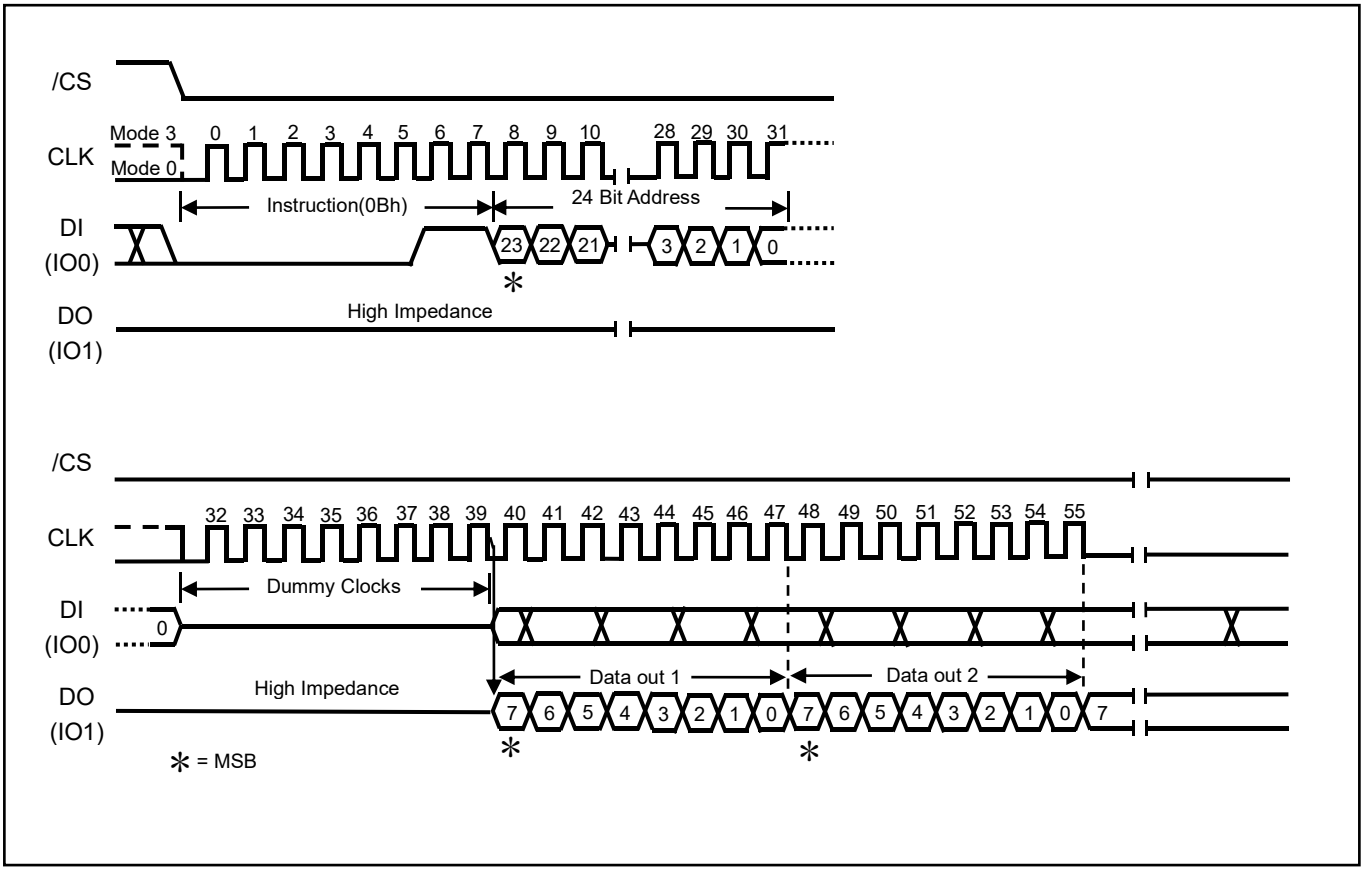


Figure 7a. Read Data Bytes at Higher Speed Sequence Diagram for SPI Mode

Fast Read (0Bh) in QPI Mode

The Fast Read instruction is also supported in QPI mode. When QPI mode is enabled, the number of dummy clocks is configured by the “Set Read Parameters (C0h)” instruction to accommodate a wide range of applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[5:4] setting, the number of dummy clocks can be configured as either 2, 4, 6 or 8. The default number of dummy clocks upon power up or after a Reset instruction is 2.

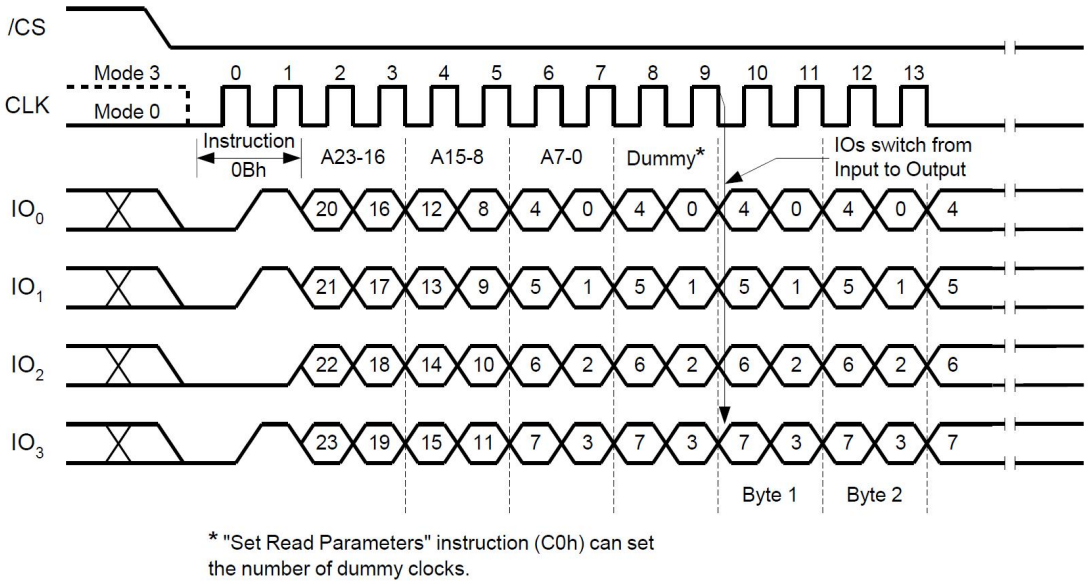


Figure 7b. Fast Read Instruction (QPI Mode)

9.10 DTR Fast Read (0Dh)

The DTR Fast Read instruction is similar to the Fast Read instruction except that the 24-bit address input and the data output require DTR (Double Transfer Rate) operation. This is accomplished by adding six “dummy” clocks after the 24-bit address as shown in Figure 8. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the DO pin is a “don’t care”.

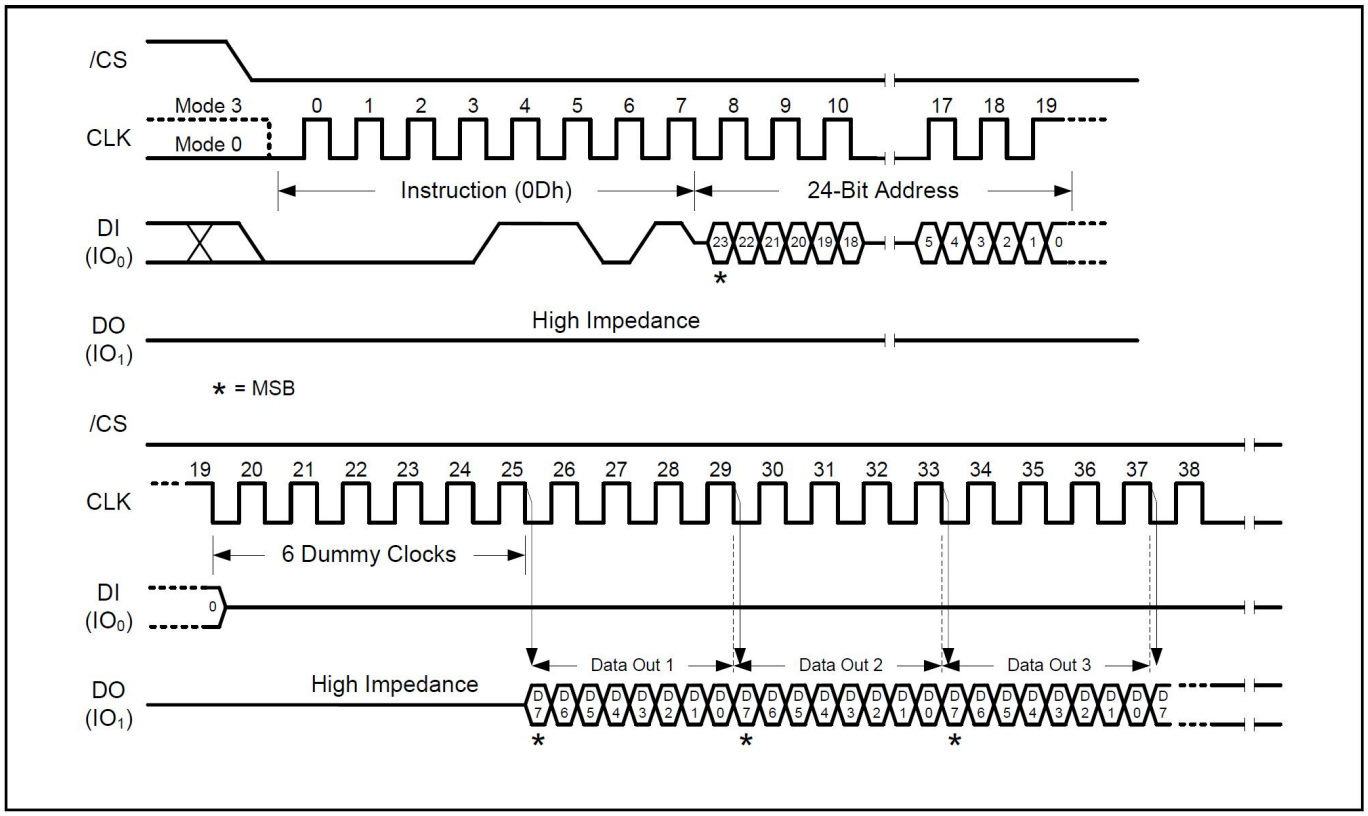


Figure 8a. DTR Fast Read Instruction (SPI Mode)

DTR Fast Read (0Dh) in QPI Mode

The DTR Fast Read instruction is also supported in QPI mode.

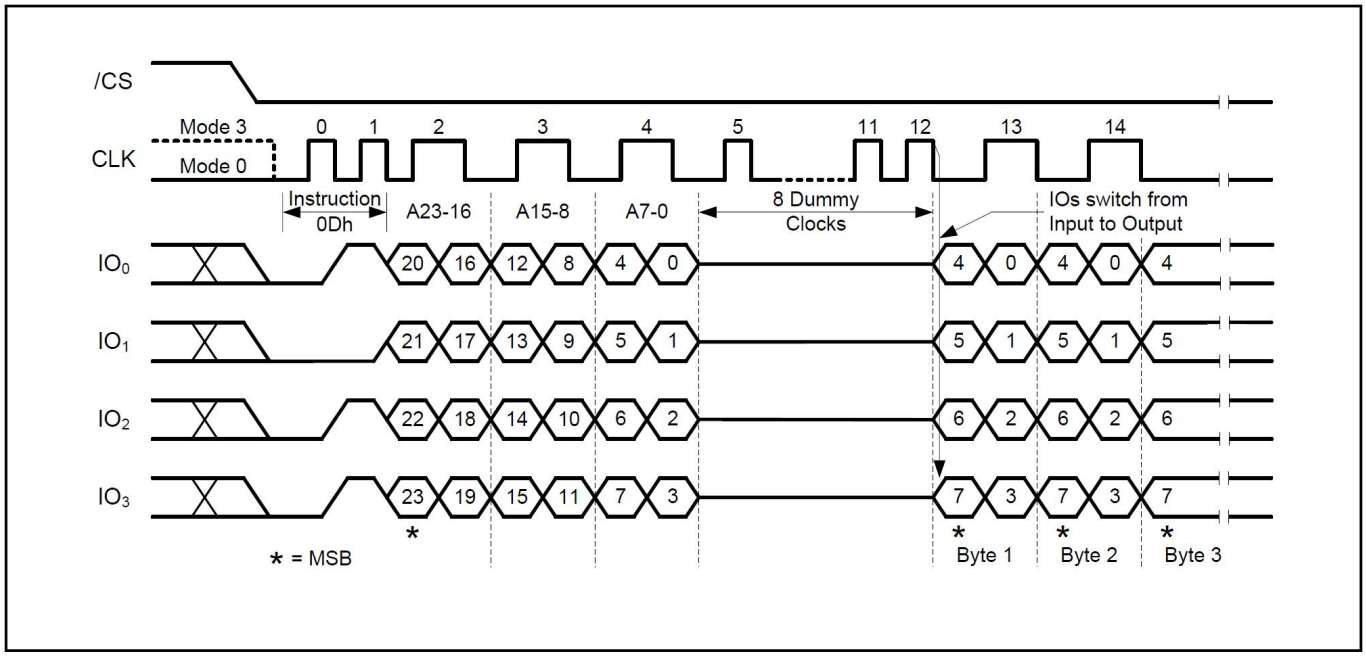


Figure 8b. DTR Fast Read Instruction (QPI Mode)

9.11 Dual Output Fast Read (3Bh)

The Fast Read Dual Output (3Bh) instruction is similar to the standard Fast Read (0Bh) instruction except that data is output on two pins; IO0 and IO1. This allows data to be transferred at twice the rate of standard SPI devices. The Fast Read Dual Output instruction is ideal for quickly downloading code from Flash to RAM upon power-up or for applications that cache code-segments to RAM for execution.

Similar to the Fast Read instruction, the Fast Read Dual Output instruction can operate at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight“dummy” clocks after the 24-bit address as shown in Figure 9. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is“don’t care”. However, the IO0 pin should be high-impedance prior to the falling edge of the first data out clock.

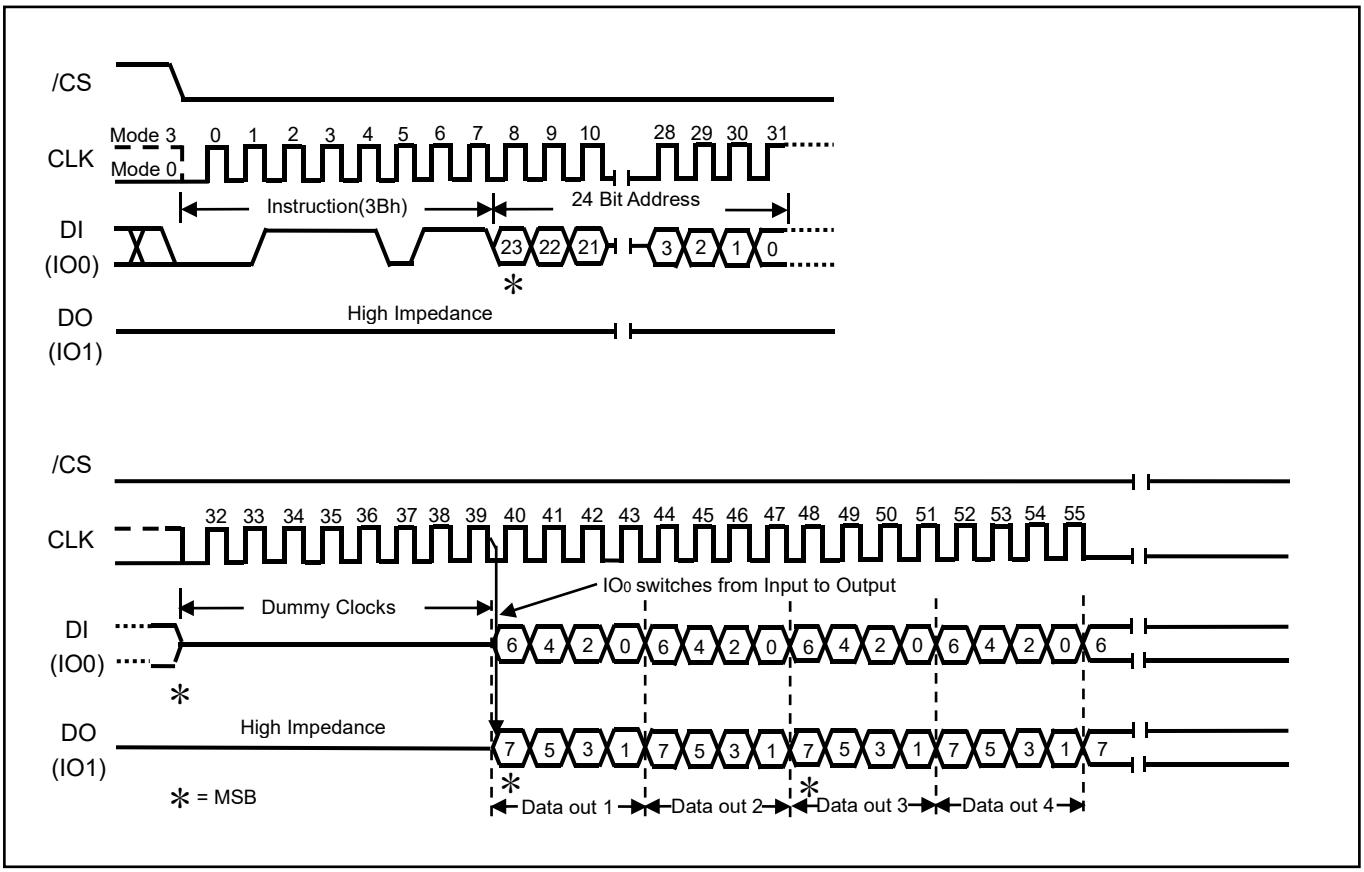


Figure 9. Dual Output Fast Read Sequence Diagram

9.12 Quad Output Fast Read (6Bh)

The Fast Read Quad Output (6Bh) instruction is similar to the Fast Read Dual Output (3Bh) instruction except that data is output on four pins, IO0, IO1, IO2, and IO3. The Quad Enable (QE) bit in Status Register-2 must be set to 1 before the device will accept the Fast Read Quad Output Instruction. The Fast Read Quad Output Instruction allows data to be transferred at four times the rate of standard SPI devices.

The Fast Read Quad Output instruction can operate at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight "dummy" clocks after the 24-bit address as shown in Figure 10. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is "don't care". However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

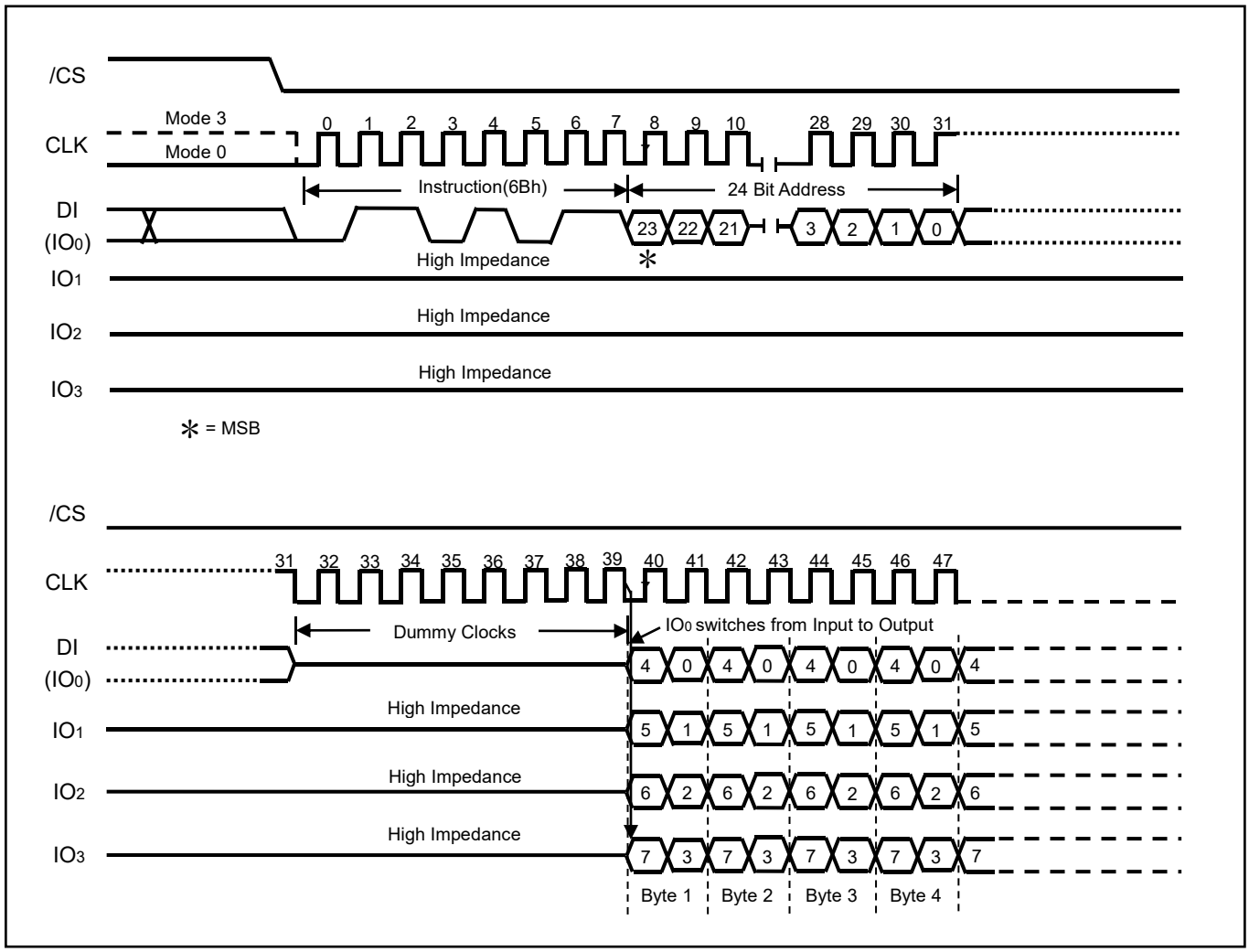


Figure 10. Quad Output Fast Read Sequence Diagram

9.13 Dual I/O Fast Read (BBH)

The Fast Read Dual I/O (BBh) instruction allows for improved random access while maintaining two IO pins, IO0 and IO1. It is similar to the Fast Read Dual Output (3Bh) instruction but with the capability to input the Address bits (A23-0) two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

Dual I/O Fast Read with"Continuous Read Mode"

The Fast Read Dual I/O instruction can further reduce instruction overhead through setting the "Read Command Bypass Mode" bits (M7-0) after the input Address bits (A23-0), as shown in Figure 11a. The upper nibble of the (M7-4) controls the length of the next Fast Read Dual I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock. If the "Read Command Bypass Mode" bits M5-4 = (1,0), then the next Fast Read Dual I/O instruction (after /CS is raised and then lowered) does not require the BBh instruction code, as shown in Figure 22b. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the "Read Command Bypass Mode" bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFFFh on IO0 for the next instruction (16 clocks), to ensure M4 = 1 and return the device to normal operation.

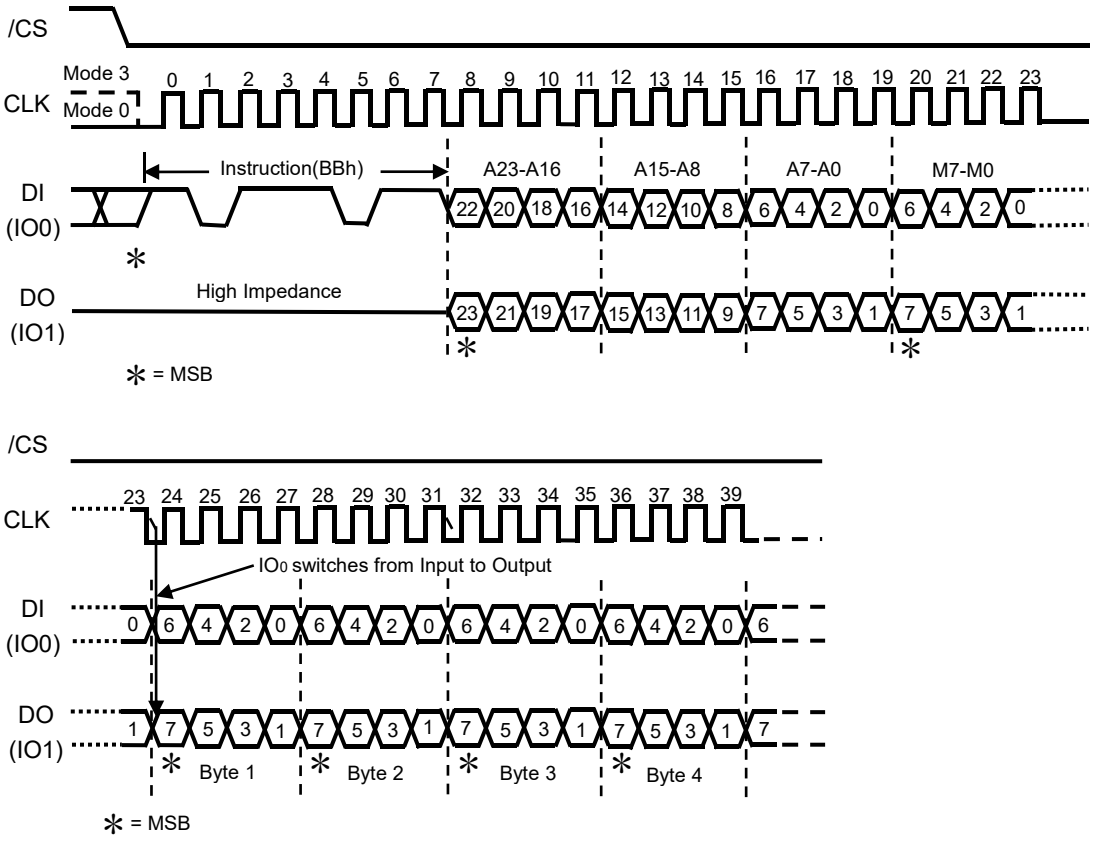


Figure 11a. Dual I/O Fast Read Sequence Diagram (M5-4≠(1, 0))

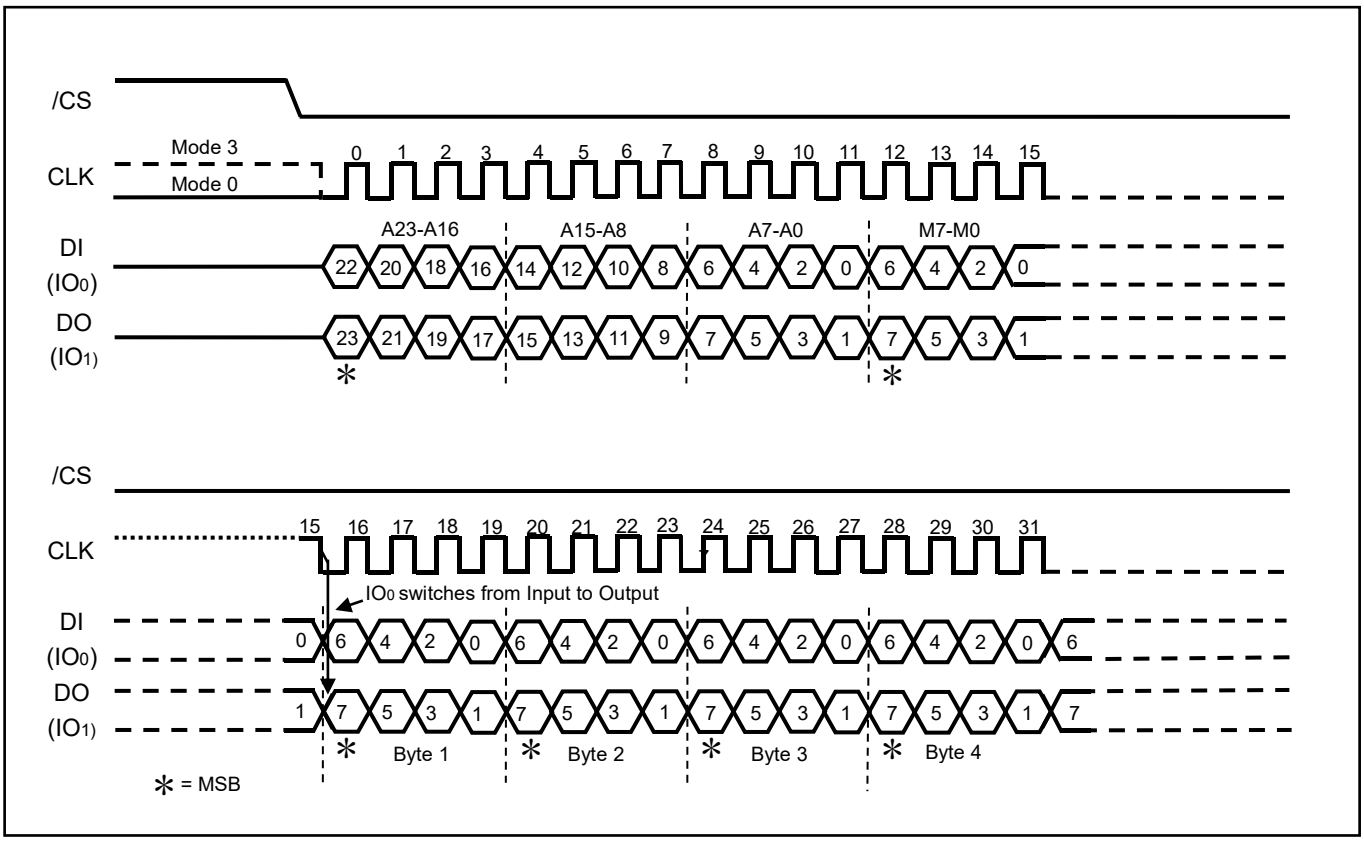


Figure 11b. Fast Read Dual I/O Instruction (Previous instruction set M5-4 = 10, SPI Mode only)

9.14 DTR Fast Read Dual I/O (BDh)

The DTR Fast Read Dual I/O (BDh) instruction allows for improved random access while maintaining two IO pins, IO0 and IO1. It is similar to the Fast Read Dual Output (3Bh) instruction but with the capability to input the Address bits (A23-0) two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

DTR Fast Read Dual I/O with "Continuous Read Mode"

The DTR Fast Read Dual I/O instruction can further reduce instruction overhead through setting the"Continuous Read Mode" bits (M7-0) after the input Address bits (A23-0), as shown in Figure 12a. The upper nibble of the (M7-4) controls the length of the next Fast Read Dual I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock. If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Dual I/O instruction (after /CS is raised and then lowered) does not require the BBh instruction code, as shown in Figure 12b. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation.

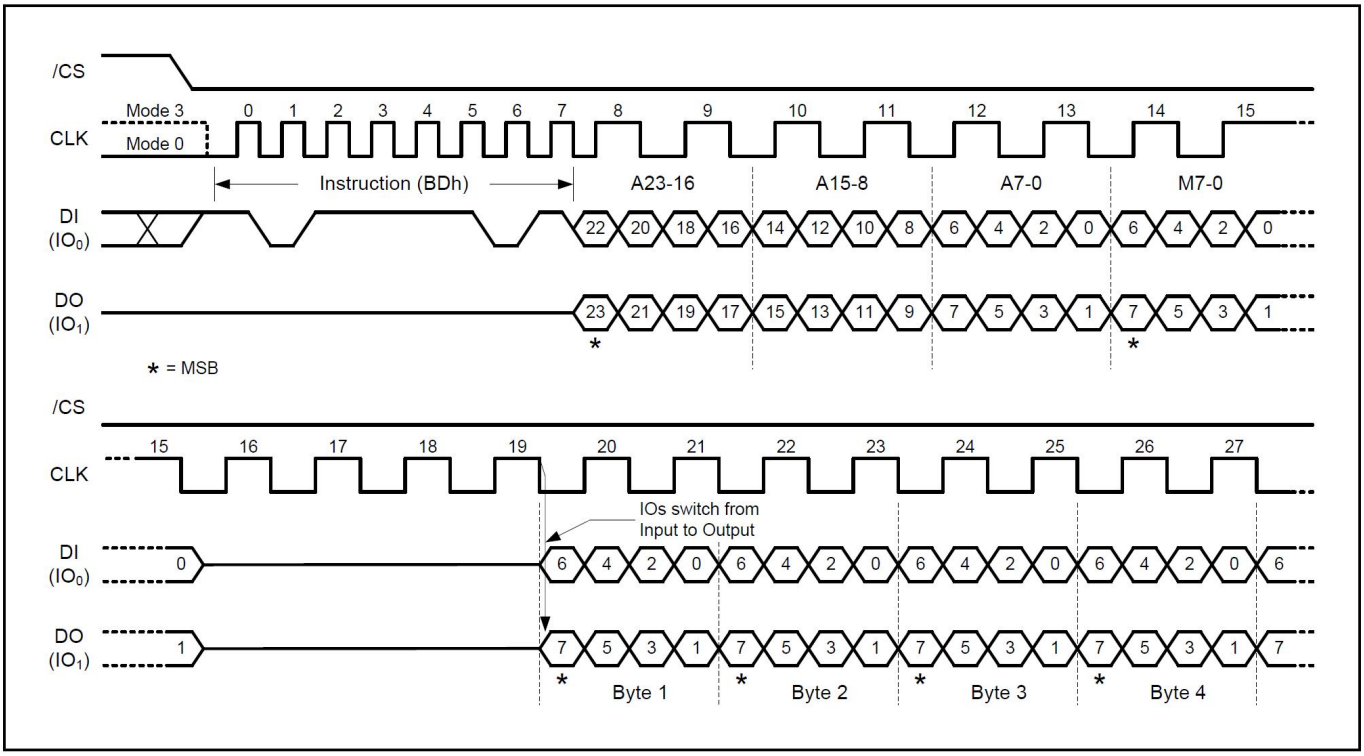


Figure 12a. DTR Fast Read Dual I/O (Initial instruction or previous M5-4≠10, SPI Mode only)

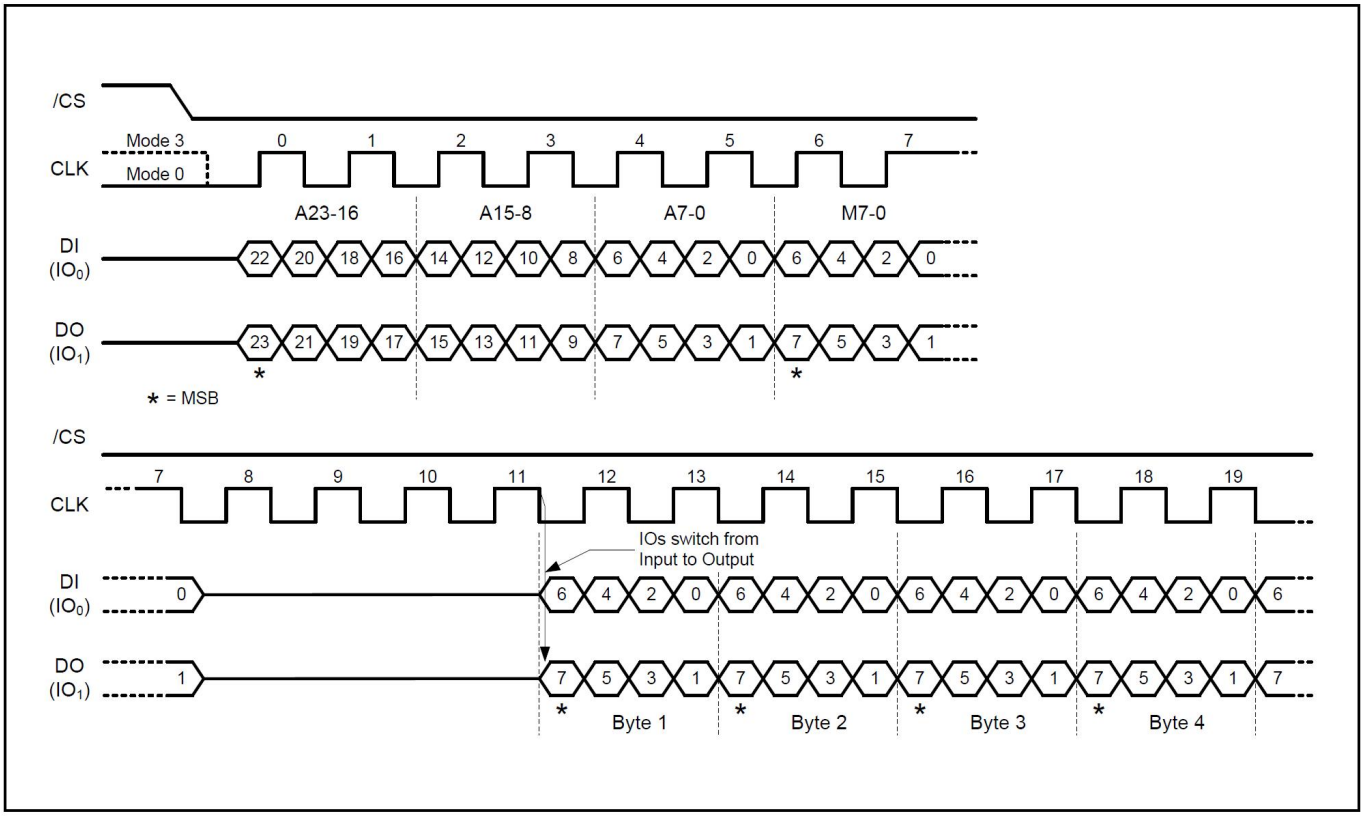


Figure 12b. DTR Fast Read Dual I/O (Previous instruction set M5-4=10, SPI Mode only)

9.15 Quad I/O Fast Read (EBH)

The Fast Read Quad I/O (EBh) instruction is similar to the Fast Read Dual I/O (BBh) instruction except that address and data bits are input and output through four pins IO0, IO1, IO2 and IO3 and four Dummy clocks are required in SPI mode prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Fast Read Quad I/O Instruction.

Quad I/O Fast Read with"Continuous Read Mode"

The Fast Read Quad I/O instruction can further reduce instruction overhead through setting the"Continuous Read Mode" bits (M7-0) after the input Address bits (A23-0), as shown in Figure 13a. The upper nibble of the (M7-4) controls the length of the next Fast Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Quad I/O instruction (after /CS is raised and then lowered) does not require the EBh instruction code, as shown in Figure 13b. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFh on IO0 for the next instruction (8 clocks), to ensure M4 = 1 and return the device to normal operation.

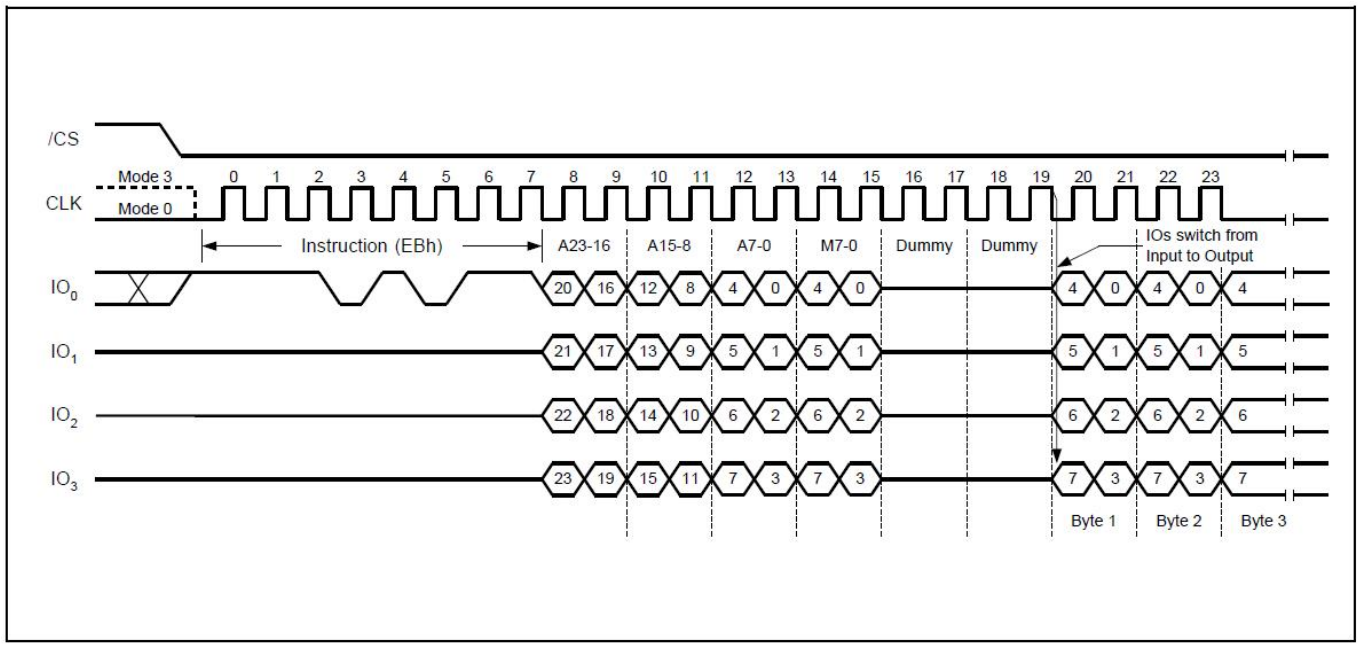


Figure 13a. Quad I/O Fast Read Sequence Diagram (M5-4≠10 SPI Mode)

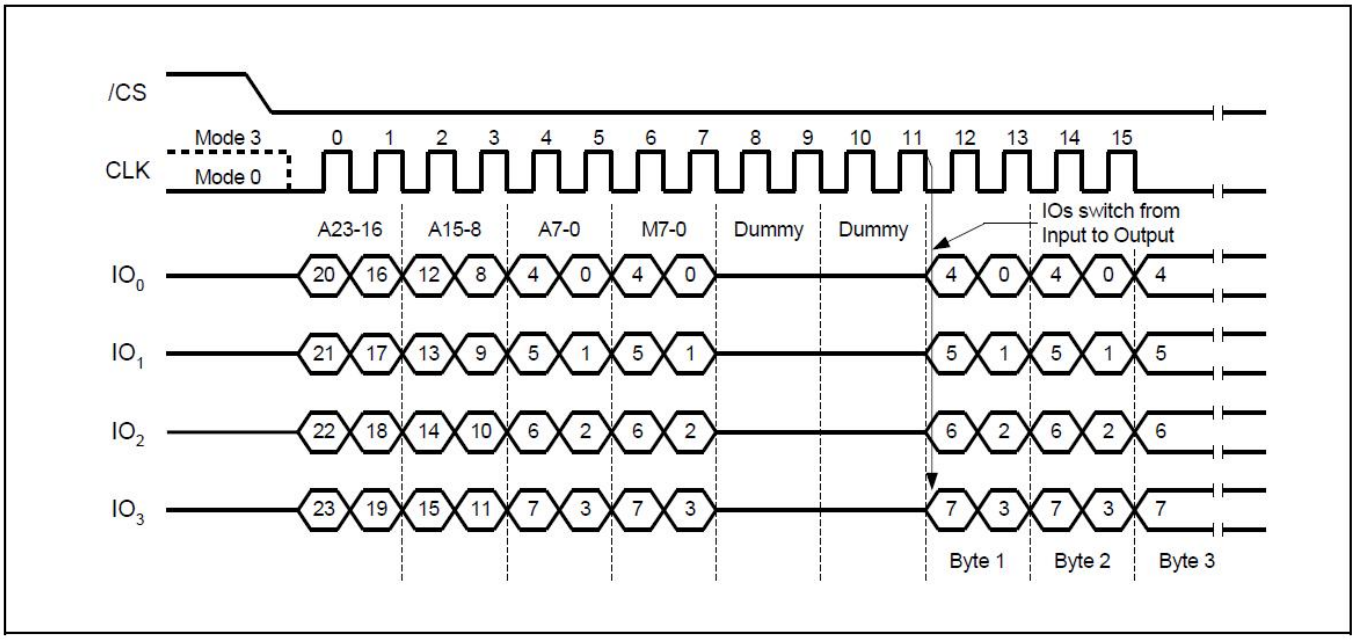


Figure 13b. Quad I/O Fast Read Sequence Diagram (M5-4= 10,SPI Mode)

Quad I/O Fast Read with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

The Fast Read Quad I/O instruction can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" (77h) command prior to EBh. The "Set Burst with Wrap" (77h) command can either enable or disable the "Wrap Around" feature for the following EBh commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands.

The "Set Burst with Wrap" instruction allows three "Wrap Bits", W6-4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-5 are used to specify the length of the wrap around section within a page. Refer to section 9.39 for detail descriptions.

Quad I/O Fast Read (EBH) in QPI mode

The Fast Read Quad I/O instruction is also supported in QPI mode, as shown in Figure 24c. When QPI mode is enabled, the number of dummy clocks is configured by the "Set Read Parameters (C0h)" instruction to accommodate a wide range of applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[5:4] setting, the number of dummy clocks can be configured as either 2, 4, 6 or 8. The default number of dummy clocks upon power up or after a Reset instruction is 2. In QPI mode, the "Read Command Bypass Mode" bits M7-0 are also considered as dummy clocks. In the default setting, the data output will follow the Read Command Bypass Mode bits immediately.

"Read Command Bypass Mode" feature is also available in QPI mode for Fast Read Quad I/O instruction. Please refer to the description on previous pages.

"Wrap Around" feature is not available in QPI mode for Fast Read Quad I/O instruction. To perform a read operation with fixed data length wrap around in QPI mode, a dedicated "Burst Read with Wrap" (0Ch) instruction must be used. Please refer to 9.39 for details.

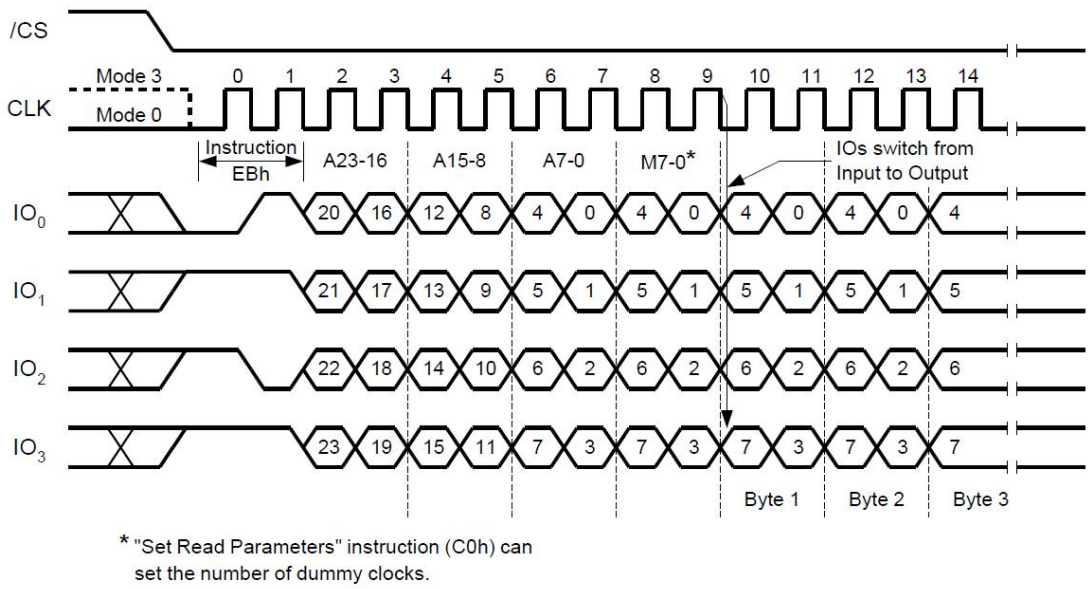


Figure 13c. Quad I/O Fast Read Sequence Diagram (M5-4≠(1, 0) QPI Mode)

9.16 DTR Fast Read Quad I/O (EDh)

The DTR Fast Read Quad I/O (EDh) instruction is similar to the Fast Read Dual I/O (BBh) instruction except that address and data bits are input and output through four pins IO0, IO1, IO2 and IO3 and 7 Dummy clocks are required in SPI mode prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Fast Read Quad I/O Instruction.

DTR Fast Read Quad I/O with "Continuous Read Mode"

The Fast Read Quad I/O instruction can further reduce instruction overhead through setting the "Read Command Bypass Mode" bits (M7-0) after the input Address bits (A23 -0), as shown in Figure 14a. The upper nibble of the (M7-4) controls the length of the next Fast Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Read Command Bypass Mode" bits M5-4 = (1,0), then the next Fast Read Quad I/O instruction (after /CS is raised and then lowered) does not require the EBh instruction code, as shown in Figure 24b. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the "Read Command Bypass Mode" bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFh/3FFh on IO0 for the next instruction (8/10 clocks), to ensure M4 = 1 and return the device to normal operation.

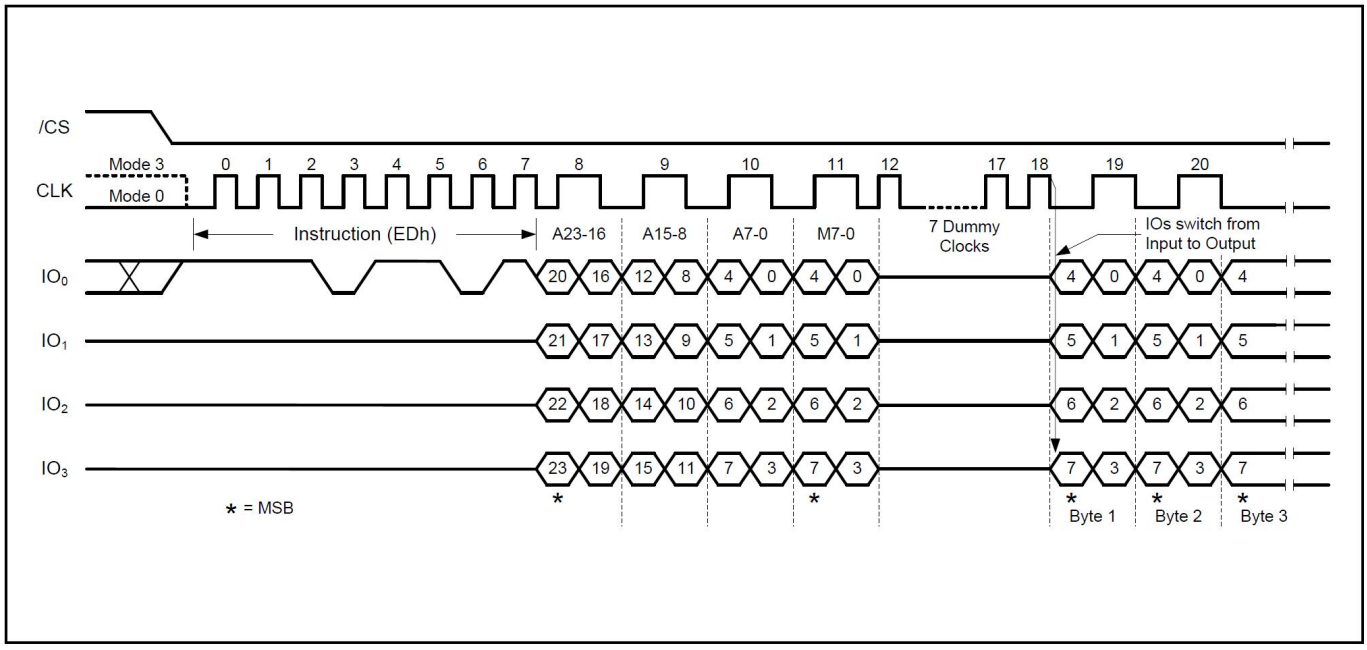


Figure 14a. DTR Fast Read Quad I/O ((M7-M0 should be set to FFh), SPI Mode)

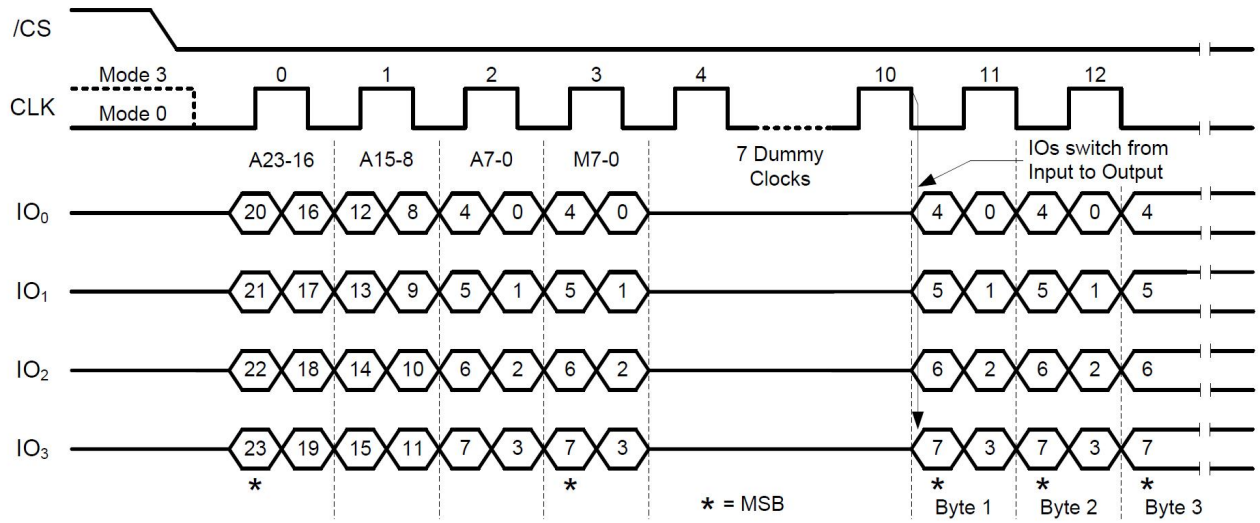


Figure 14b. Fast Read Quad I/O (Previous instruction set M5-4=10, SPI Mode)

DTR Fast Read Quad I/O with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

The Fast Read Quad I/O instruction can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" (77h) command prior to EDh. The "Set Burst with Wrap" (77h) command can either enable or disable the "Wrap Around" feature for the following EDh commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands.

The "Set Burst with Wrap" instruction allows three "Wrap Bits", W6-4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-5 are used to specify the length of the wrap around section within a page. Refer to section 9.39 for detail descriptions.

DTR Fast Read Quad I/O (EDh) in QPI Mode

The DTR Fast Read Quad I/O instruction is also supported in QPI mode, as shown in Figure 19c. In QPI mode, the "Read Command Bypass Mode" bits M7-0 are also considered as dummy clocks. In the default setting, the data output will follow the Read Command Bypass Mode bits immediately.

"Read Command Bypass Mode" feature is also available in QPI mode for Fast Read Quad I/O instruction. Please refer to the description on previous pages.

"Wrap Around" feature is not available in QPI mode for Fast Read Quad I/O instruction. To perform a read operation with fixed data length wrap around in QPI mode, a dedicated "Burst Read with Wrap" (0Ch) instruction must be used. Please refer to 9.39 for details.

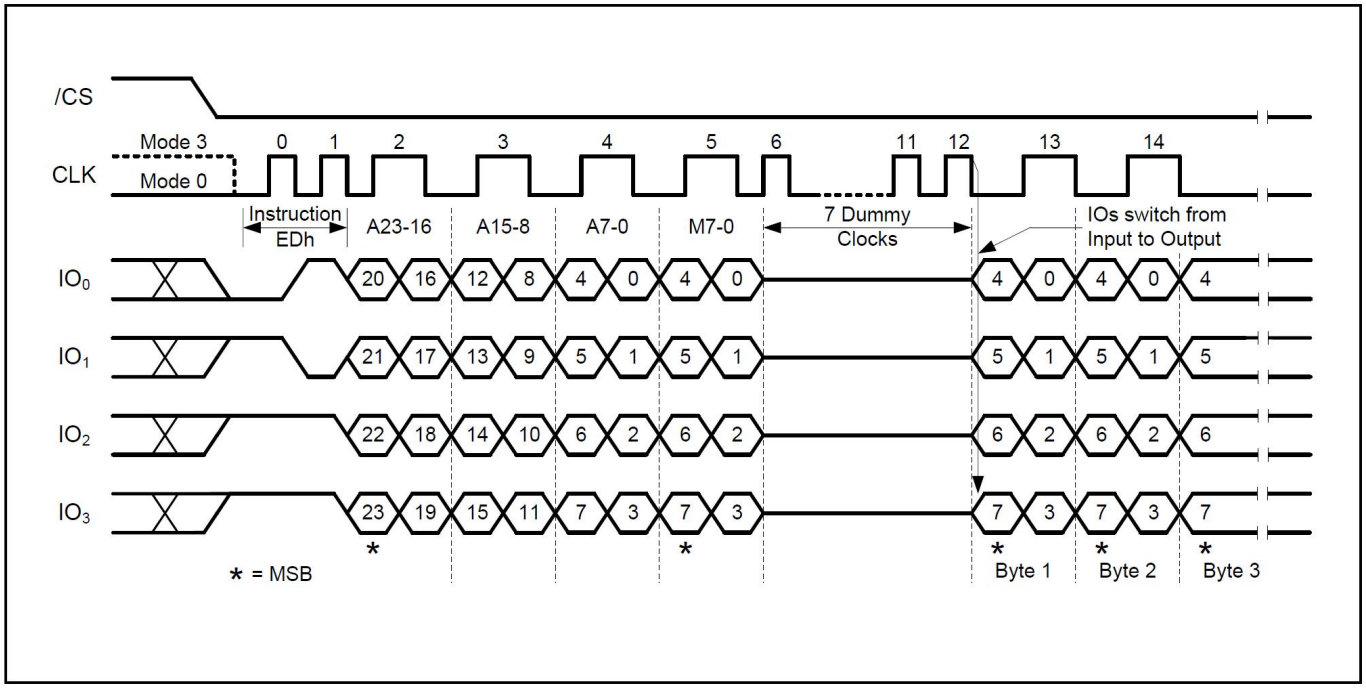


Figure 14c. DTR Fast Read Quad I/O (Initial instruction or previous M5-4≠10, QPI Mode)

9.17 Set Burst with Wrap (77H)

In Standard SPI mode, the Set Burst with Wrap (77h) instruction is used in conjunction with "Fast Read Quad I/O" instructions to access a fixed length of 8/16/32/64-byte section within a 256-byte page. Certain applications can benefit from this feature and improve the overall system code execution performance.

Similar to a Quad I/O instruction, the Set Burst with Wrap instruction is initiated by driving the /CS pin low and then shifting the instruction code "77h" followed by 24 dummy bits and 8 "Wrap Bits", W7-0. The instruction sequence is shown in Figure 31. Wrap bit W7 and the lower nibble W3-0 are not used.

W6,W5	W4=0		W4=1 (Default)	
	Wrap Around	Wrap Length	Wrap Around	Wrap Length
0, 0	Yes	8-byte	No	N/A
0, 1	Yes	16-byte	No	N/A
1, 0	Yes	32-byte	No	N/A
1, 1	Yes	64-byte	No	N/A

Once W6-4 is set by a Set Burst with Wrap instruction, all the following "Fast Read Quad I/O" instructions will use the W6-4 setting to access the 8/16/32/64-byte section within any page. To exit the "Wrap Around" function and return to normal read operation, another Set Burst with Wrap instruction should be issued to set W4 = 1. The default value of W4 upon power on or after a software/hardware reset is 1.

In QPI mode, the "Burst Read with Wrap (0Ch)" instruction should be used to perform the Read operation with "Wrap Around" feature. The Wrap Length set by W5-4 in Standard SPI mode is still valid in QPI mode and can also be re-configured by "Set Read Parameters (C0h)" instruction.

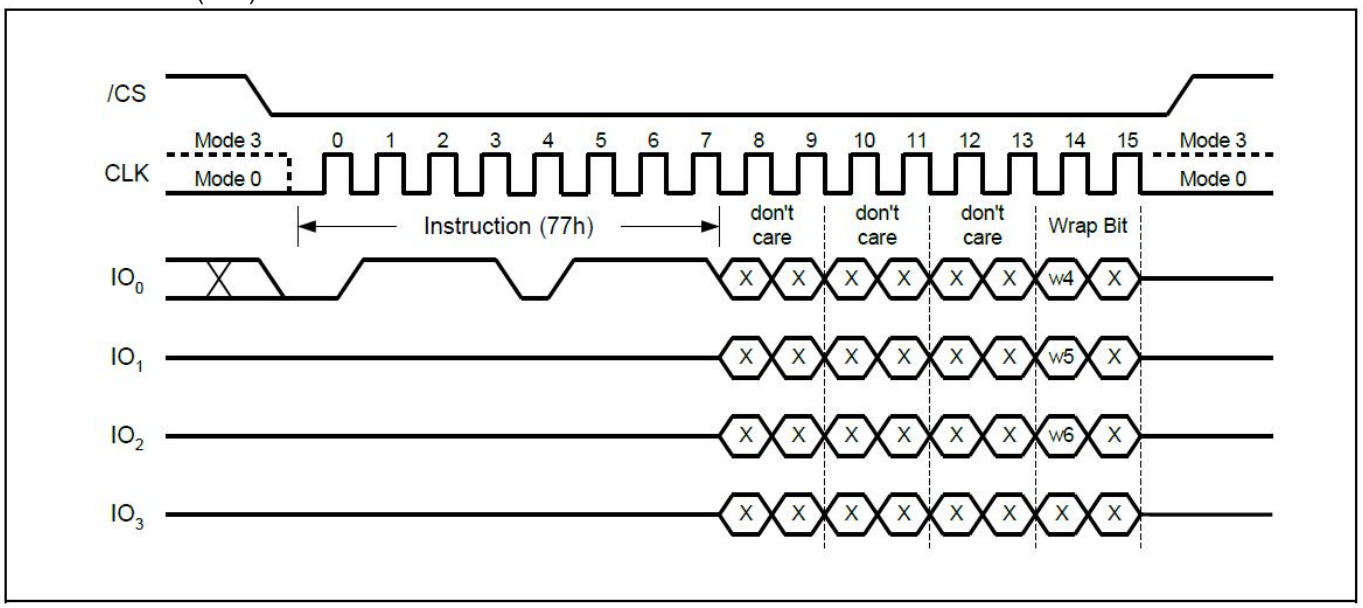


Figure 15 Set Burst with Wrap Sequence Diagram(SPI Mode only)

9.18 Page Program (PP) (02H)

The Page Program instruction allows from one byte to 256 bytes (a page) of data to be programmed at previously erased (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Page Program Instruction (Status Register bit WEL= 1). The instruction is initiated by driving the /CS pin low then shifting the instruction code "02h" followed by a 24-bit address (A23-A0) and at least one data byte, into the DI pin. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. The Page Program instruction sequence is shown in Figure 16.

If an entire 256 byte page is to be programmed, the last address byte (the 8 least significant address bits) should be set to 0. If the last address byte is not zero, and the number of clocks exceeds the remaining page length, the addressing will wrap to the beginning of the page. In some cases, less than 256 bytes (a partial page) can be programmed without having any effect on other bytes within the same page. One condition to perform a partial page program is that the number of clocks cannot exceed the remaining page length. If more than 256 bytes are sent to the device the addressing will wrap to the beginning of the page and overwrite previously sent data.

As with the write and erase instructions, the /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Page Program instruction will not be executed. After /CS is driven high, the self-timed Page Program instruction will commence for a time duration of tpp (See AC Characteristics). While the Page Program cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Page Program cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Page Program instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits or the Individual Block/Sector Locks.

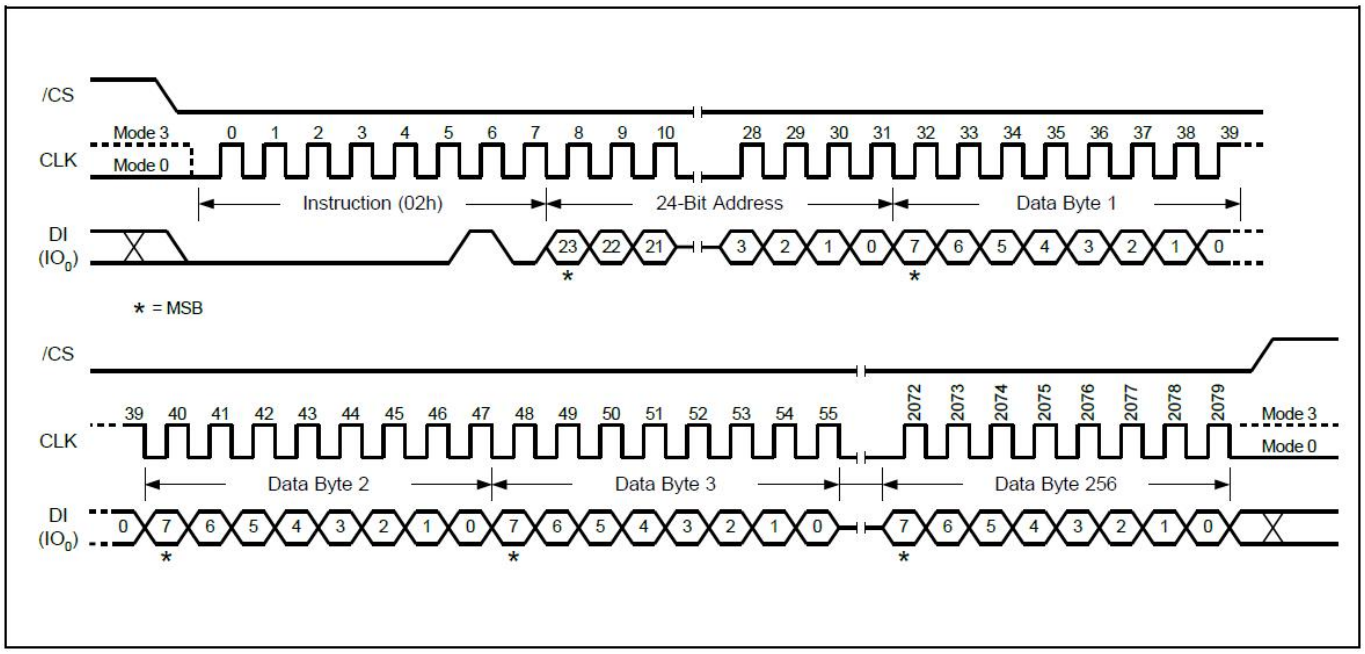


Figure 16a Page Program Sequence Diagram for SPI Mode

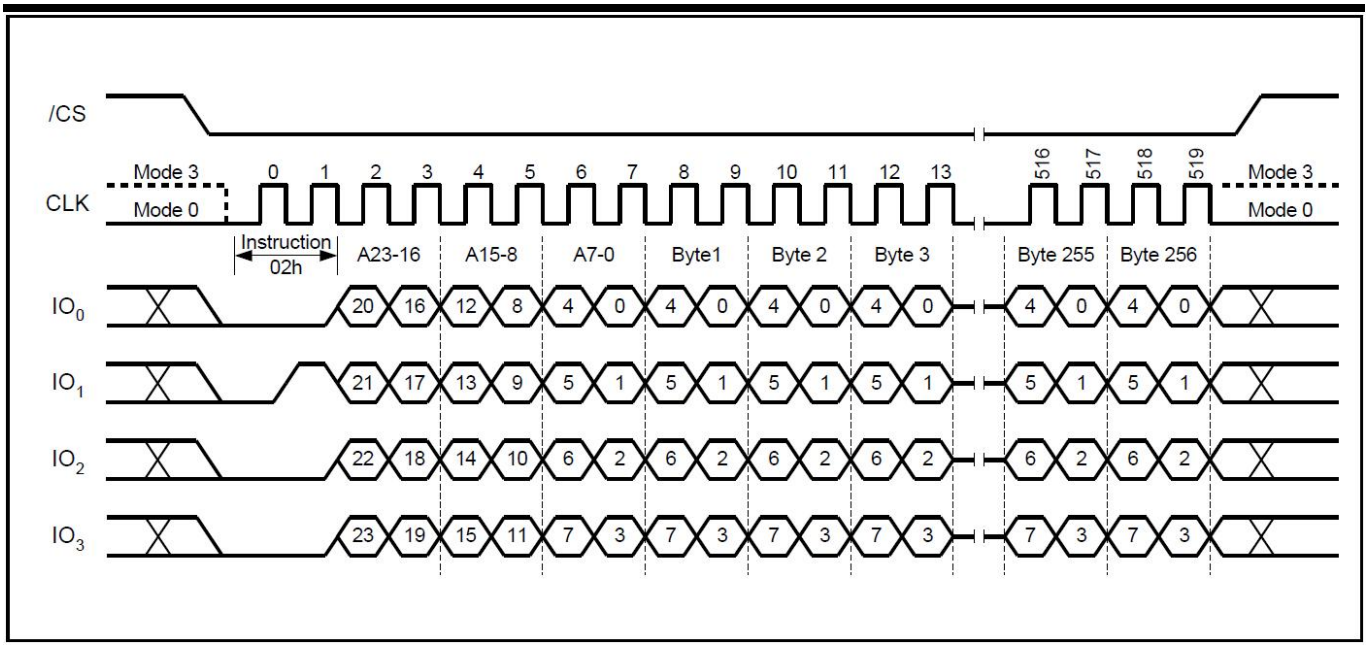


Figure 16b Page Program Sequence Diagram for QPI Mode

9.19 Quad Page Program (32H)

The Quad Page Program instruction allows up to 256 bytes of data to be programmed at previously erased (FFh) memory locations using four pins: IO0, IO1, IO2, and IO3. The Quad Page Program can improve performance for PROM Programmer and applications that have slow clock speeds <5MHz. Systems with faster clock speed will not realize much benefit for the Quad Page Program instruction since the inherent page program time is much greater than the time it take to clock-in the data.

To use Quad Page Program the Quad Enable (QE) bit in Status Register-2 must be set to 1. A Write Enable instruction must be executed before the device will accept the Quad Page Program instruction (Status Register-1, WEL=1). The instruction is initiated by driving the /CS pin low then shifting the instruction code "32h" followed by a 24-bit address (A23-A0) and at least one data byte, into the IO pins. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. All other functions of Quad Page Program are identical to standard Page Program. The Quad Page Program instruction sequence is shown in Figure 17.

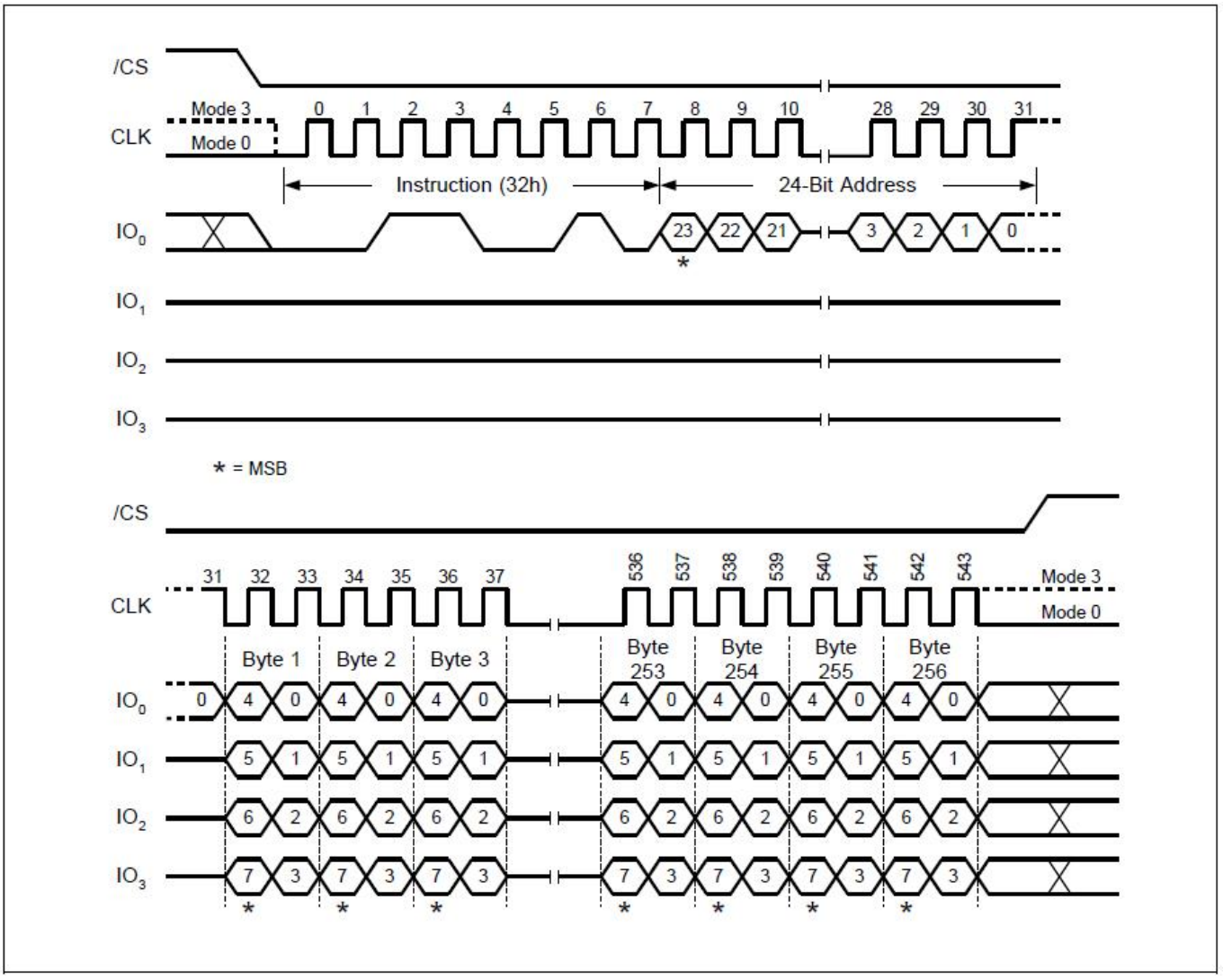


Figure 17 Quad Page Program Sequence Diagram

9.20 Sector Erase (SE) (20H)

The Sector Erase instruction sets all memory within a specified sector (4K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Sector Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code "20h" followed a 24-bit sector address (A23-A0). The Sector Erase instruction sequence is shown in Figure 31a & 31b.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Sector Erase instruction will not be executed. After /CS is driven high, the self-timed Sector Erase instruction will commence for a time duration of tSE (See AC Characteristics). While the Sector Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Sector Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Sector Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Sector Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits or the Individual Block/Sector Locks.

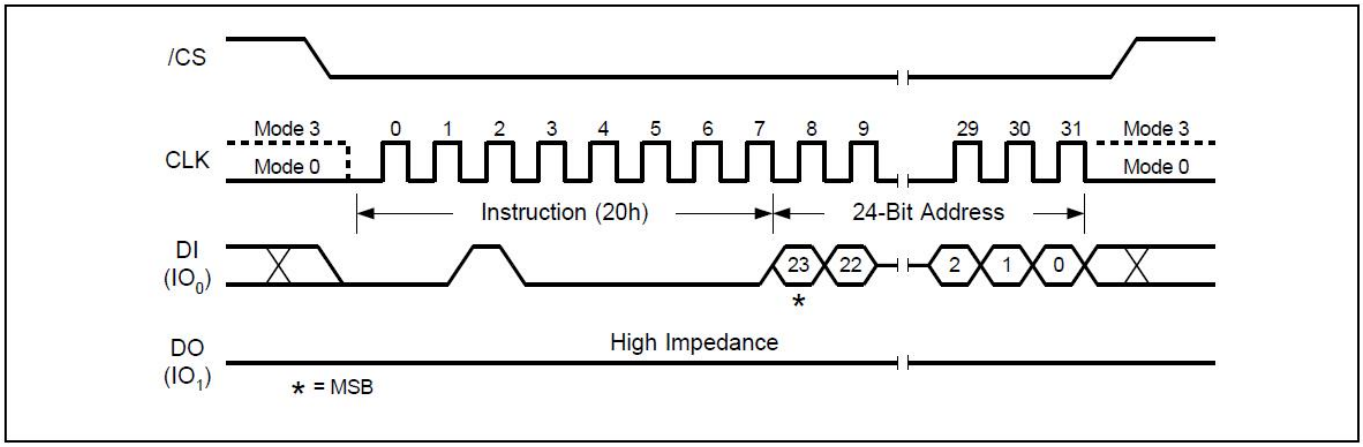


Figure18a. Sector Erase Sequence Diagram for SPI Mode

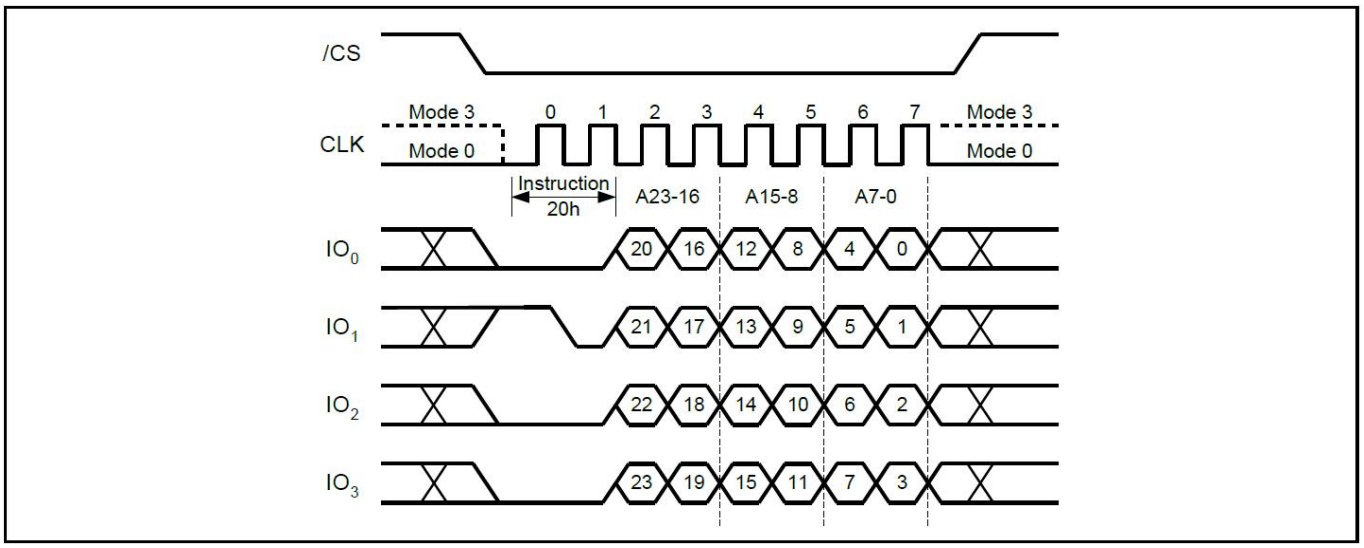


Figure 18b. Sector Erase Sequence Diagram for QPI Mode

9.21 32KB Block Erase (BE) (52H)

The Block Erase instruction sets all memory within a specified block (32K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code "52h" followed a 24-bit block address (A23-A0). The Block Erase instruction sequence is shown in Figure 19a & 19b.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After /CS is driven high, the self-timed Block Erase instruction will commence for a time duration of tBE1 (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits or the Individual Block/Sector Locks.

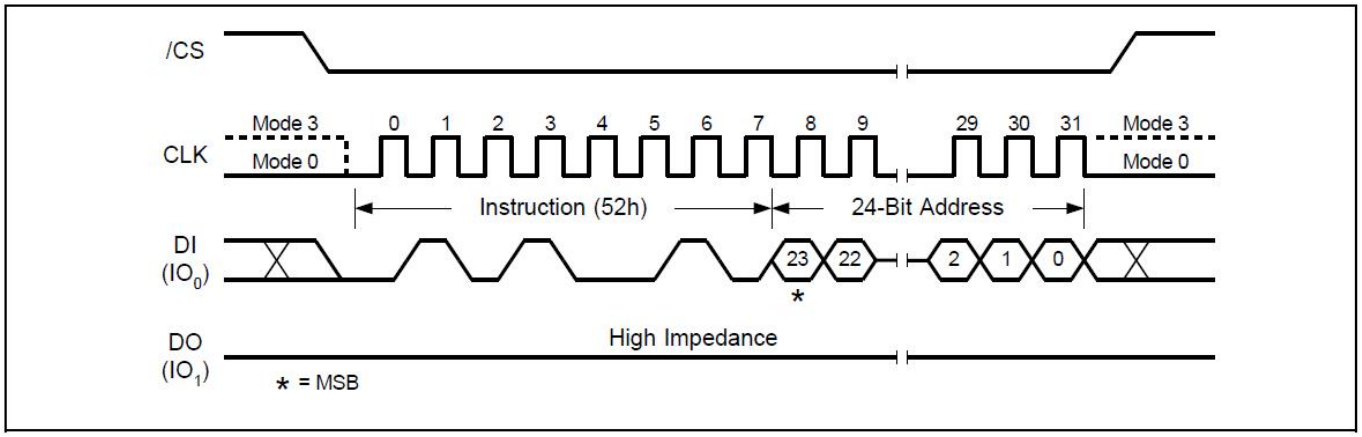


Figure 19a. 32KB Block Erase Sequence Diagram for SPI Mode

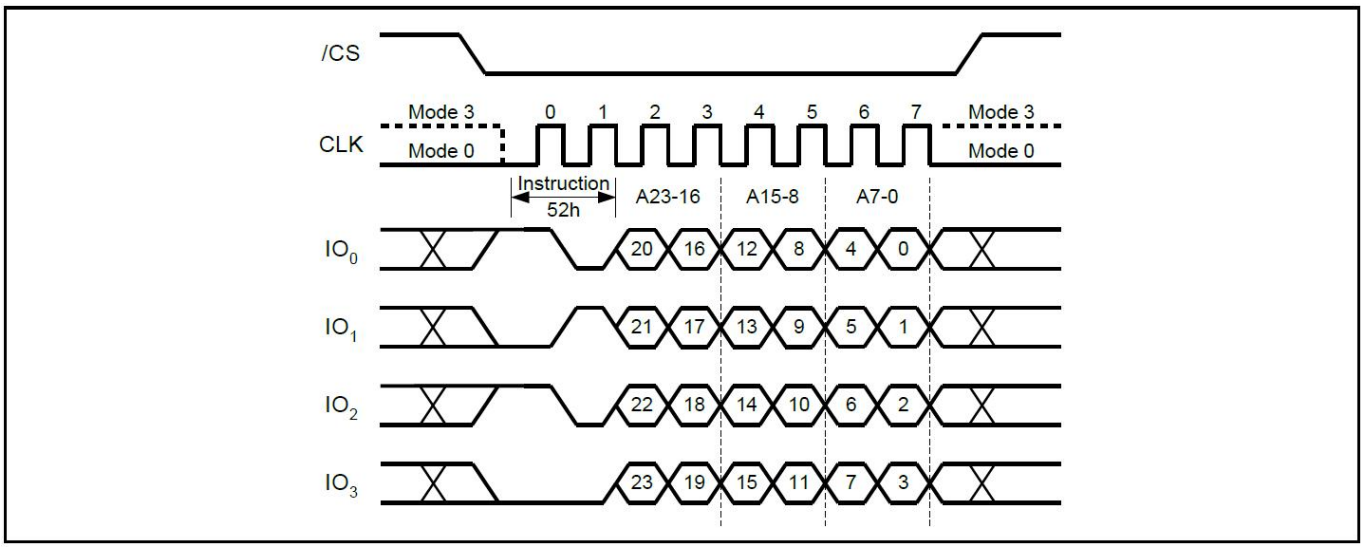


Figure 19b. 32KB Block Erase Sequence Diagram for QPI Mode

9.22 64KB Block Erase (BE) (D8H)

The Block Erase instruction sets all memory within a specified block (64K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code "D8h" followed a 24-bit block address (A23-A0). The Block Erase instruction sequence is shown in Figure 20a & 20b.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After /CS is driven high, the self-timed Block Erase instruction will commence for a time duration of tBE (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits or the Individual Block/Sector Locks.

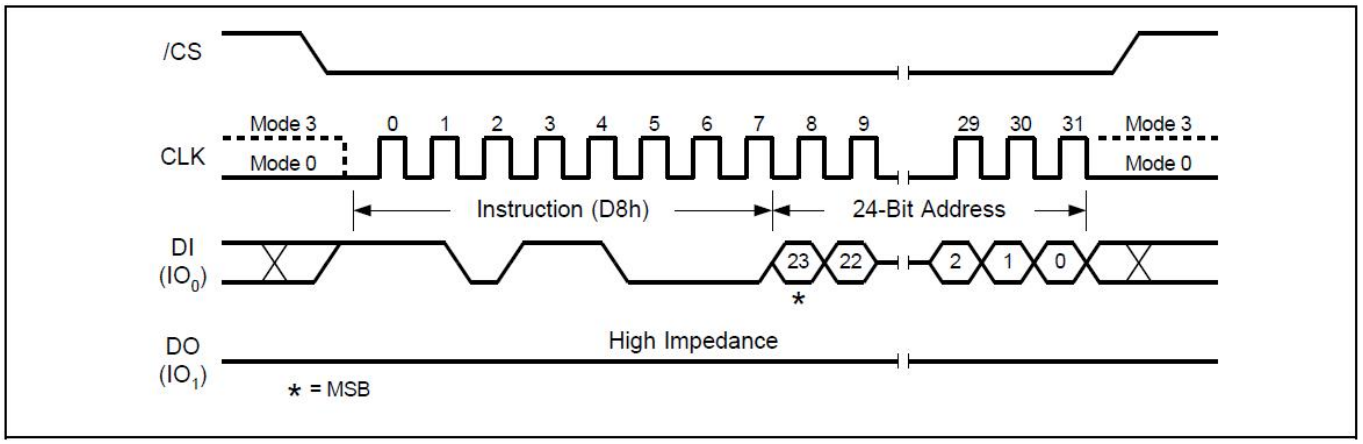


Figure 20a 64KB Block Erase Sequence Diagram for SPI Mode

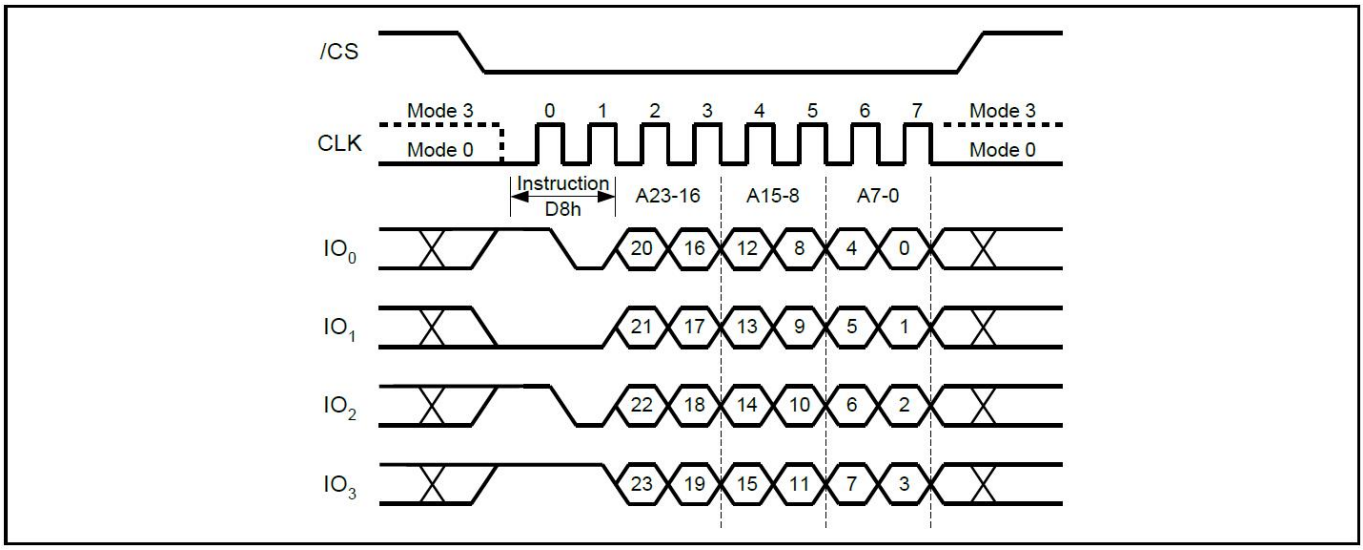


Figure 20b. 64KB Block Erase Sequence Diagram for QPI Mode

9.23 Chip Erase (CE) (60/C7H)

The Chip Erase instruction sets all memory within the device to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Chip Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code "C7h" or "60h". The Chip Erase instruction sequence is shown in Figure 21.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Chip Erase instruction will not be executed. After /CS is driven high, the self-timed Chip Erase instruction will commence for a time duration of tCE (See AC Characteristics). While the Chip Erase cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Chip Erase cycle and becomes a 0 when finished and the device is ready to accept other instructions again. After the Chip Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Chip Erase instruction will not be executed if any memory region is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits or the Individual Block/Sector Locks.

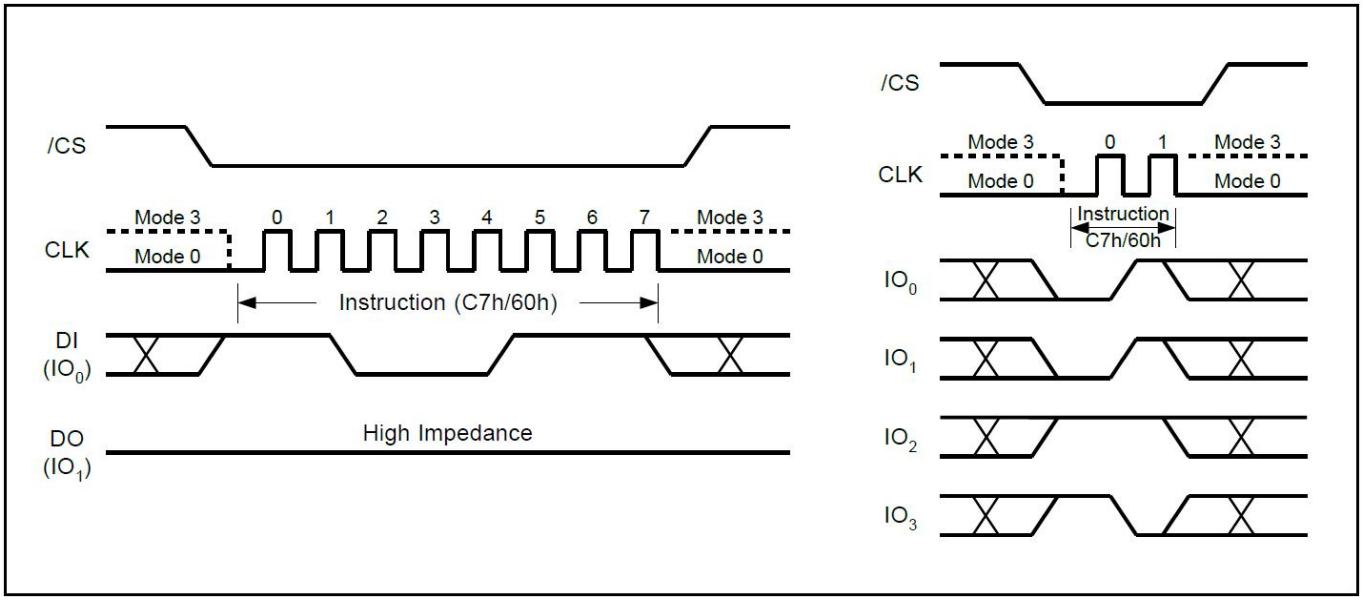


Figure 21. Chip Erase Sequence Diagram for SPI Mode(left) or QPI Mode(right)

9.24 Deep Power-Down (DP) (B9H)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Power-down instruction. The lower power consumption makes the Power-down instruction especially useful for battery powered applications (See ICC1 and ICC2 in AC Characteristics). The instruction is initiated by driving the /CS pin low and shifting the instruction code "B9h" as shown in Figure 22a & 22b.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Power-down instruction will not be executed. After /CS is driven high, the power-down state will entered within the time duration of tDP (See AC Characteristics). While in the power-down state only the Release Power-down /Device ID (ABh) instruction, which restores the device to normal operation, will be recognized. All other instructions are ignored. This includes the Read Status Register instruction, which is always available during normal operation. Ignoring all but one instruction makes the Power Down state a useful condition for securing maximum write protection. The device always powers-up in the normal operation with the standby current of ICC1.

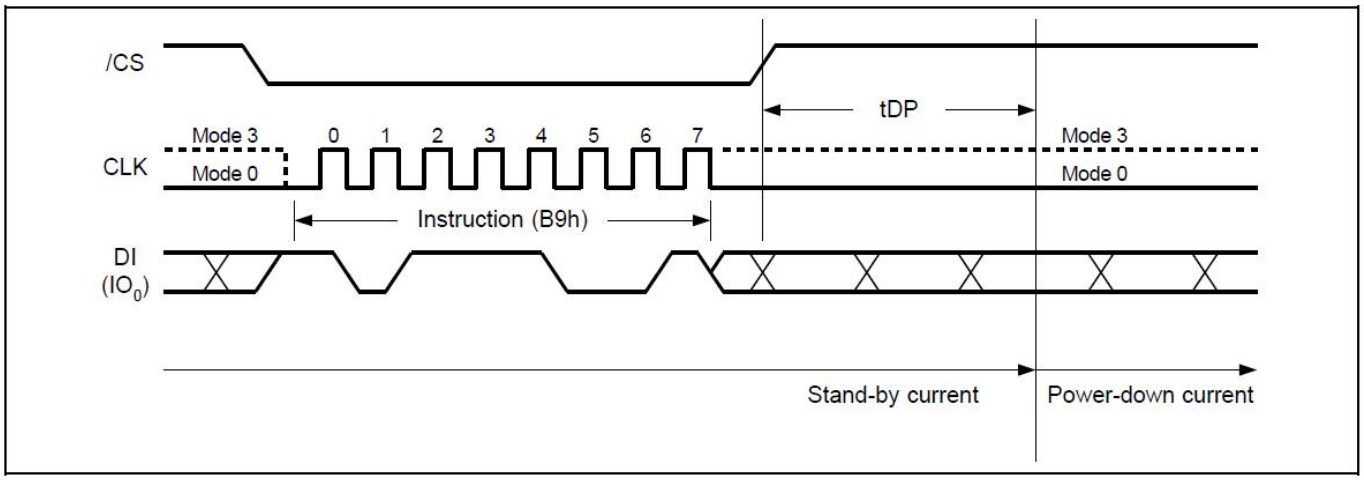


Figure 22a. Deep Power-Down Sequence Diagram for SPI Mode

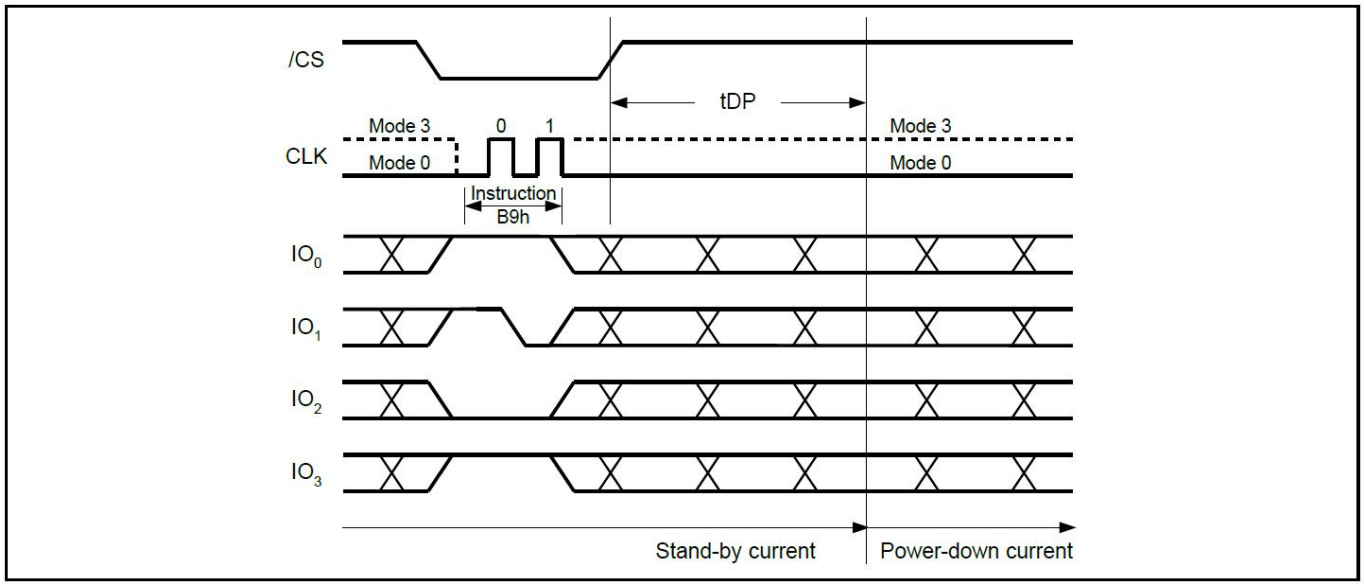


Figure 22b. Deep Power-Down Sequence Diagram for QPI Mode

9.25 Release from Deep Power-Down and Read Device ID (RDI) (ABH)

The Release from Power-Down and Read Device ID command is a multi-purpose command. It can be used to release the device from the Power-Down state or obtain the devices electronic identification (ID) number.

To release the device from the Power-Down state, the command is issued by driving the CS# pin low, shifting the instruction code "ABH" and driving CS# high as shown in Figure23. Release from Power-Down will take the time duration of tRES1 (See AC Characteristics) before the device will resume normal operation and other command are accepted. The CS# pin must remain high during the tRES1 time duration.

When used only to obtain the Device ID while not in the Power-Down state, the command is initiated by driving the CS# pin low and shifting the instruction code "ABH" followed by 3-dummy byte. The Device ID bits are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure37. The Device ID value is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The command is completed by driving CS# high.

If the Release from Power-down instruction is issued while an Erase, Program or Write cycle is in process (when BUSY equals 1) the instruction is ignored and will not have any effects on the current cycle.

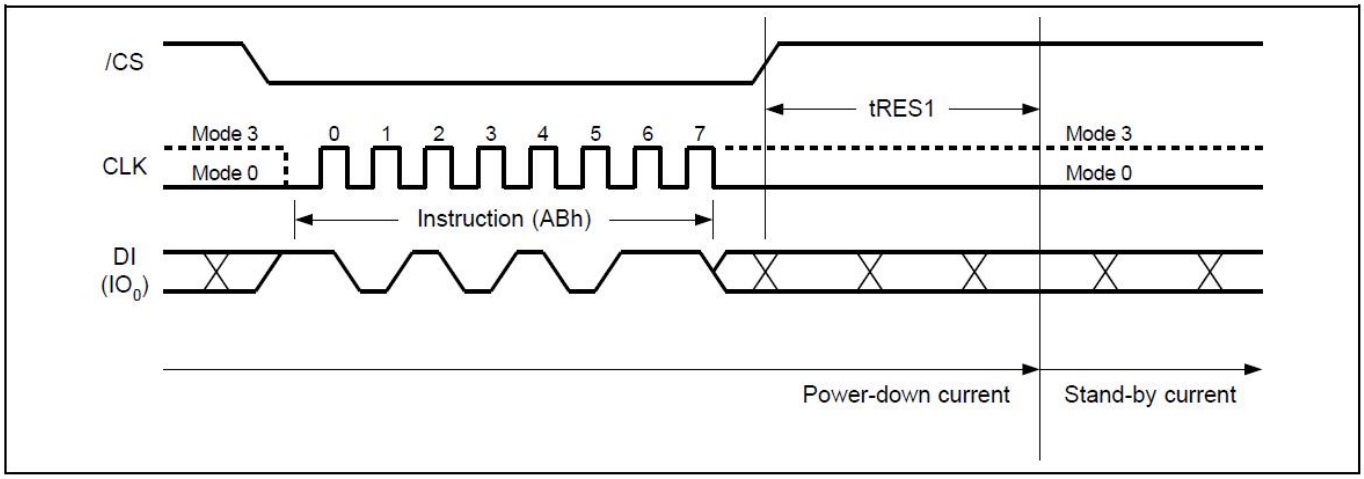


Figure 23a. Release Power-Down Sequence Diagram for SPI Mode

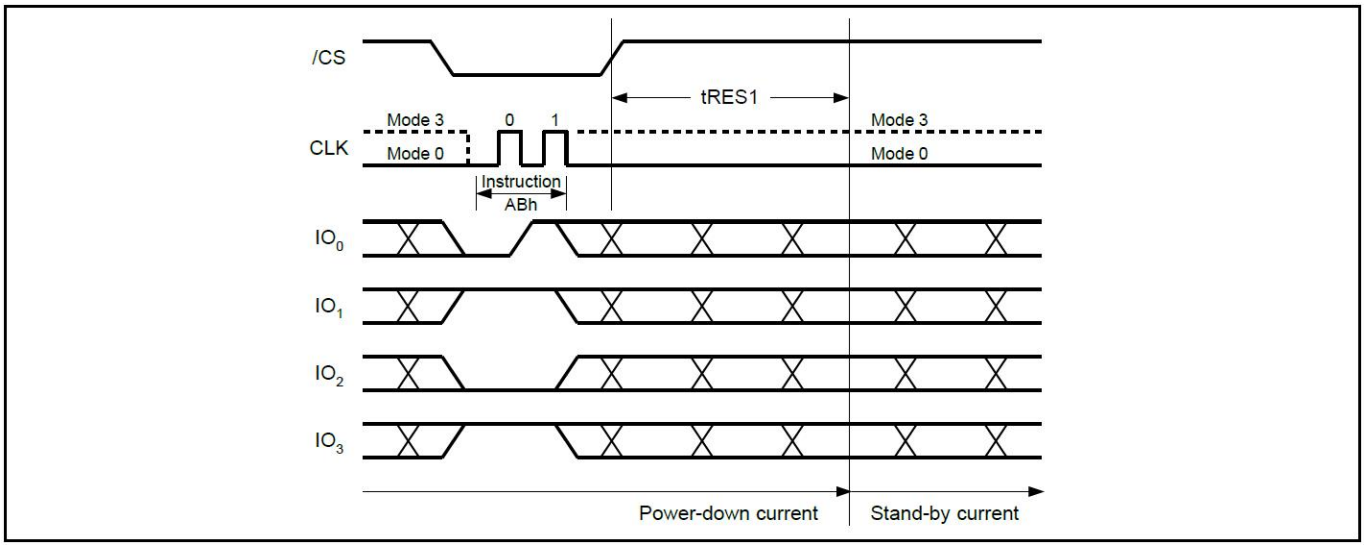


Figure 23b. Release Power-Down Sequence Diagram for QPI Mode

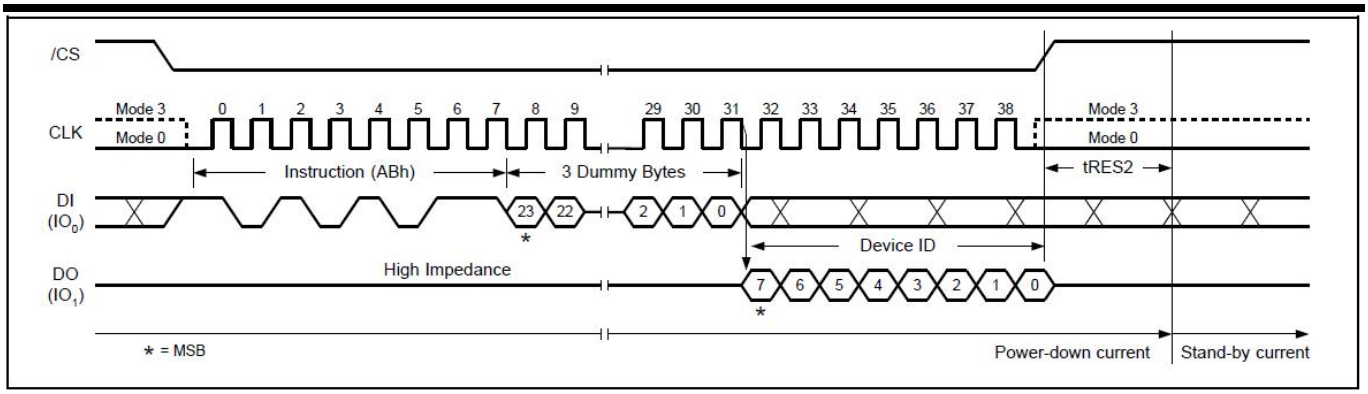


Figure 23c. Release Power-Down/Read Device ID Sequence Diagram for SPI Mode

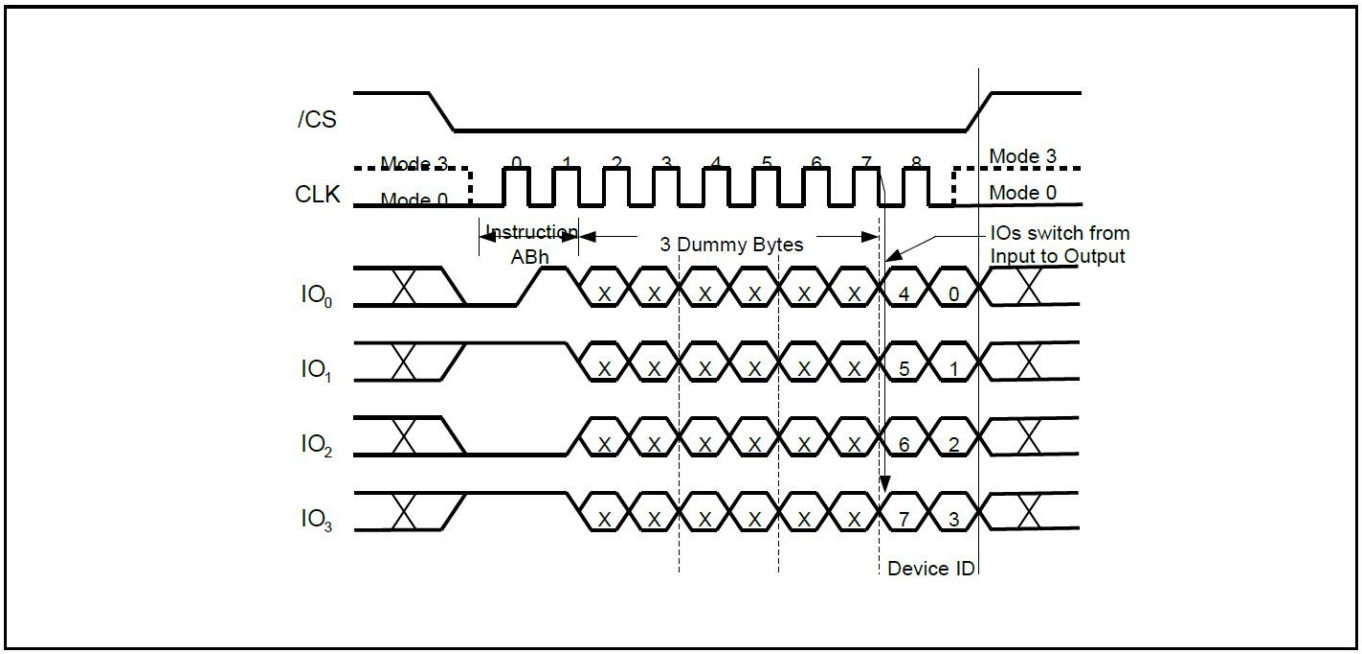


Figure 23d. Release Power-Down/Read Device ID Sequence Diagram for QPI Mode

9.26 Read Manufacture Id/ Device Id (REMS) (90H)

The Read Manufacturer/Device ID command is an alternative to the Release from Power-Down / Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID.

The command is initiated by driving the CS# pin low and shifting the command code "90H" followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure23. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

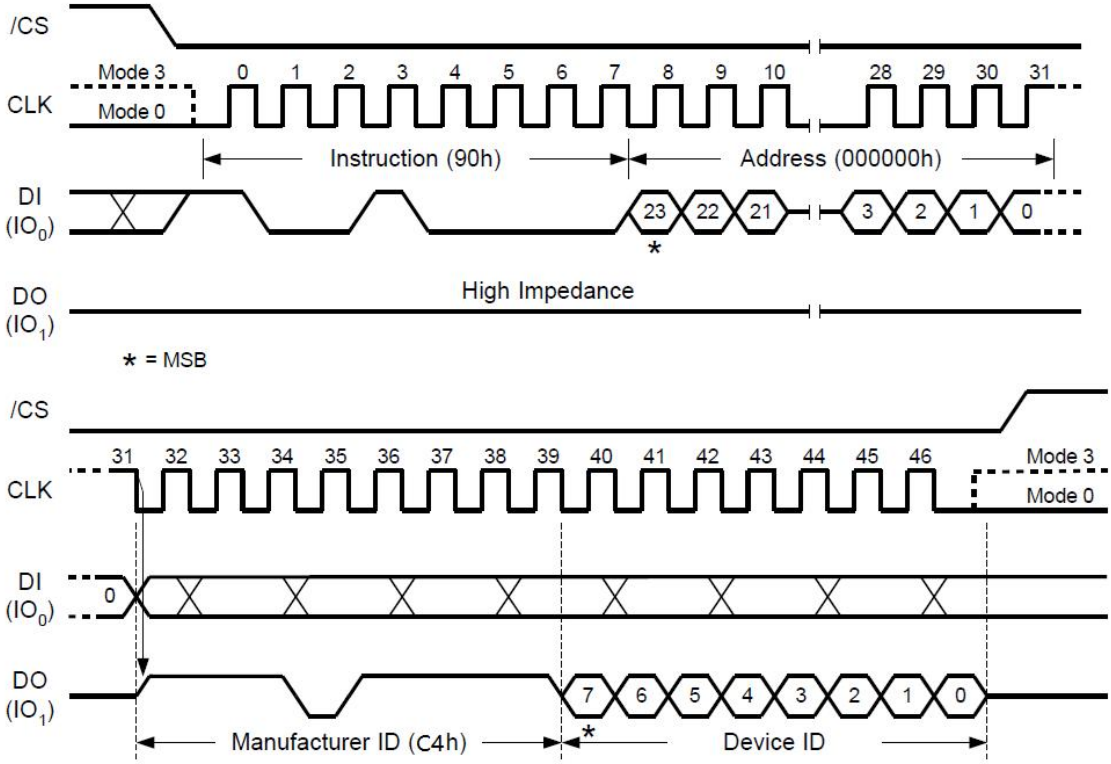


Figure 24a. Read Manufacture ID/ Device ID Sequence Diagram for SPI Mode

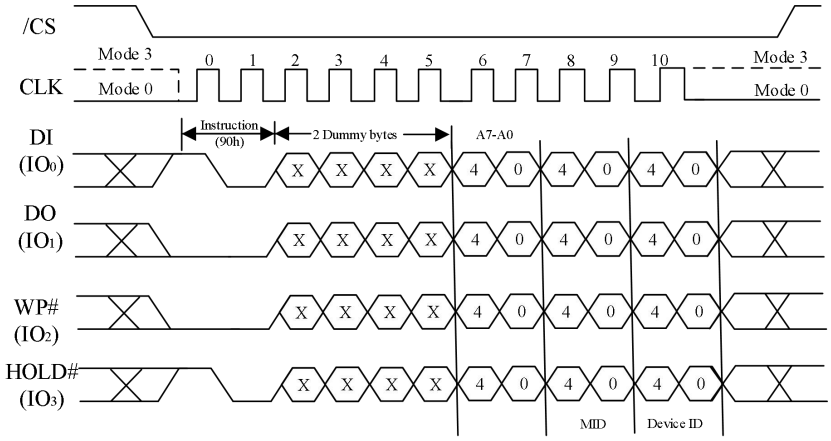


Figure 24b. Read Manufacture ID/ Device ID Sequence Diagram for QPI Mode

9.27 Read Manufacture ID/ Device ID Dual I/O (92H)

The Read Manufacturer / Device ID Dual I/O instruction is an alternative to the Read Manufacturer / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID at 2x speed.

The Read Manufacturer / Device ID Dual I/O instruction is similar to the Fast Read Dual I/O instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code "92h" followed by a 24-bit address (A23-A0) of 000000h, but with the capability to input the Address bits two bits per clock. After which, the Manufacturer ID for Giantec (C4h) and the Device ID are shifted out 2 bits per clock on the falling edge of CLK with most significant bits (MSB) first as shown in Figure 40. The Device ID values for the GT25Q16BL are listed in Manufacturer and Device Identification table. If the 24-bit address is initially set to 000001h the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving /CS high.

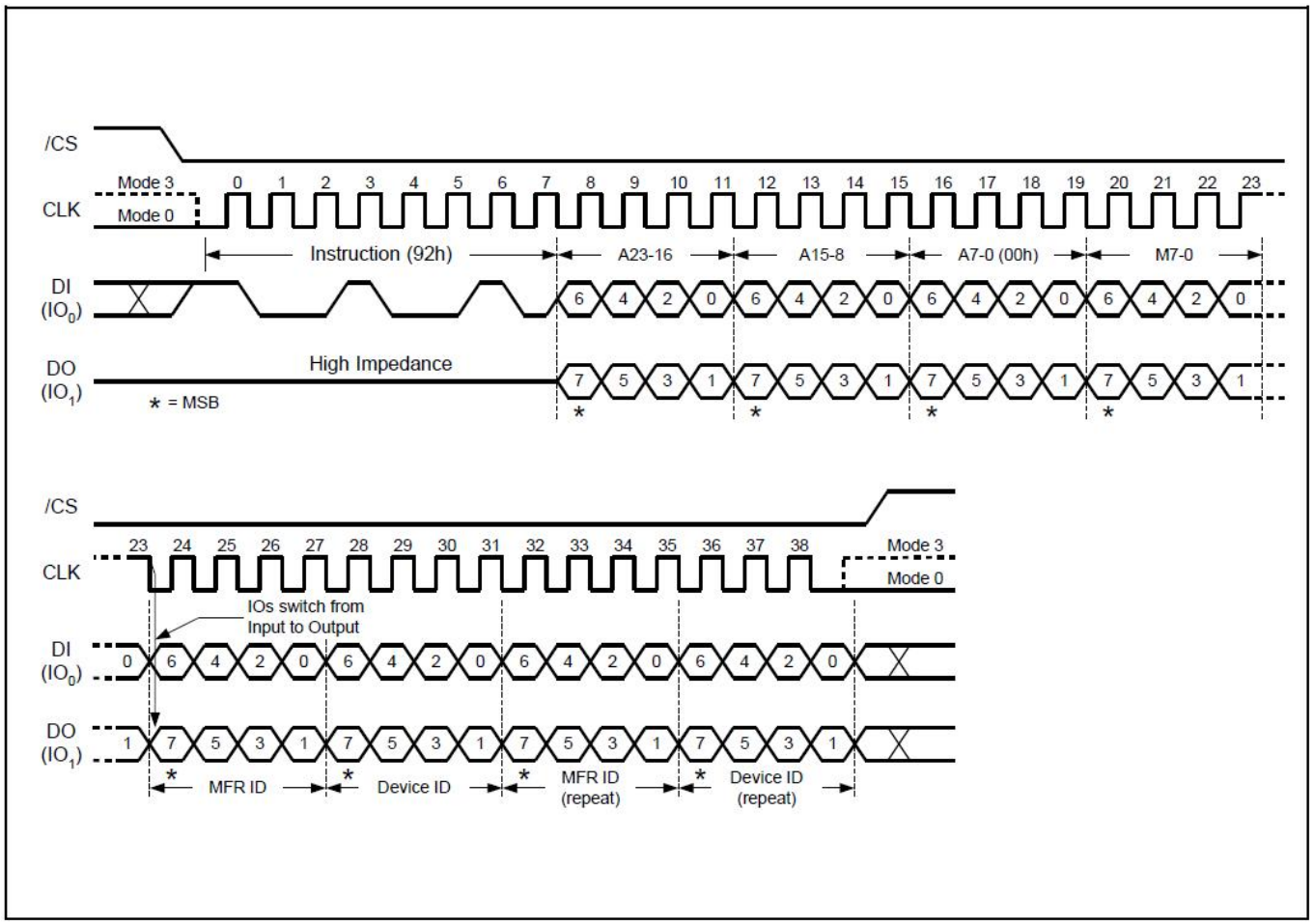


Figure 24. Read Manufacture ID/ Device ID Dual I/O Sequence Diagram

9.28 Read Manufacture ID/ Device ID Quad I/O (94H)

The Read Manufacturer / Device ID Quad I/O instruction is an alternative to the Read Manufacturer / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID at 4x speed.

The Read Manufacturer / Device ID Quad I/O instruction is similar to the Fast Read Quad I/O instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code "94h" followed by a four clock dummy cycles and then a 24-bit address (A23-A0) of 000000h, but with the capability to input the Address bits four bits per clock. After which, the Manufacturer ID for Giantec (C4h) and the Device ID are shifted out four bits per clock on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 41. The Device ID values for the GT25Q16BL are listed in Manufacturer and Device Identification table. If the 24-bit address is initially set to 000001h the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving /CS high.

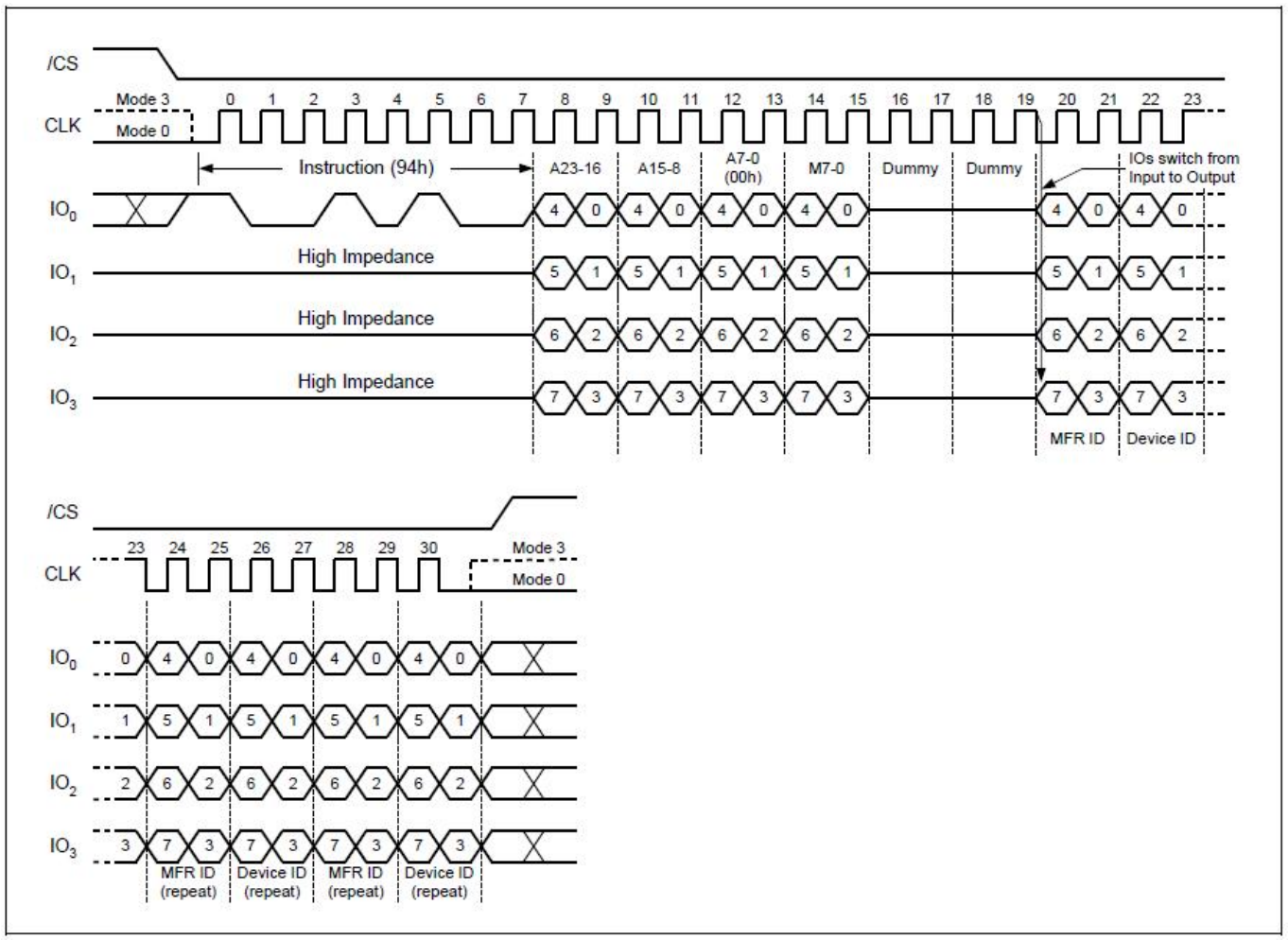


Figure 25. Read Manufacture ID/ Device ID Quad I/O Sequence Diagram

9.29 Read Identification (RDID) (9FH)

For compatibility reasons, the GT25Q16BL provides several instructions to electronically determine the identity of the device. The Read JEDEC ID instruction is compatible with the JEDEC standard for SPI compatible serial memories that was adopted in 2003. The instruction is initiated by driving the /CS pin low and shifting the instruction code "9Fh". The JEDEC assigned Manufacturer ID byte for Giantec (C4h) and two Device ID bytes, Memory Type (ID15-ID8) and Capacity (ID7-ID0) are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 26a & 26b. For memory type and capacity values refer to Manufacturer and Device Identification table.

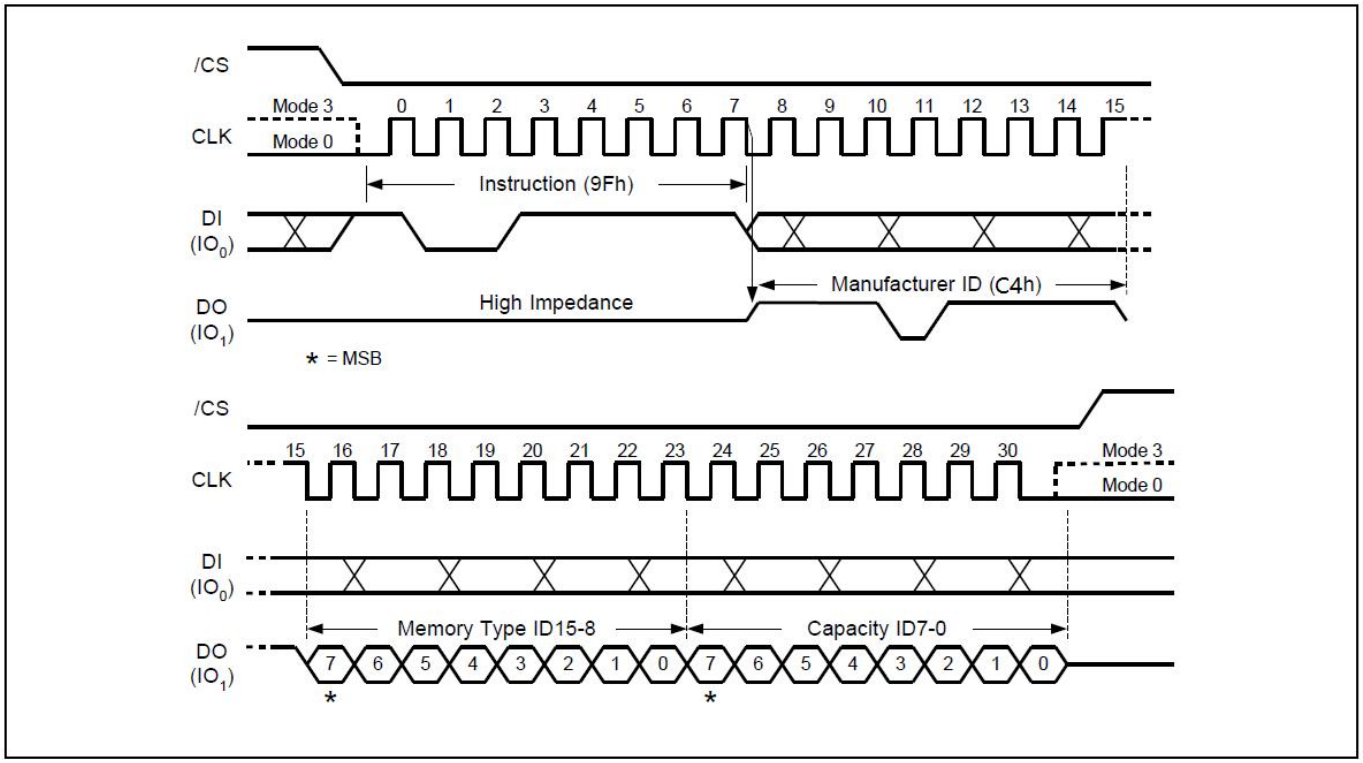


Figure 26a.Read Identification ID Sequence Diagram for SPI Mode

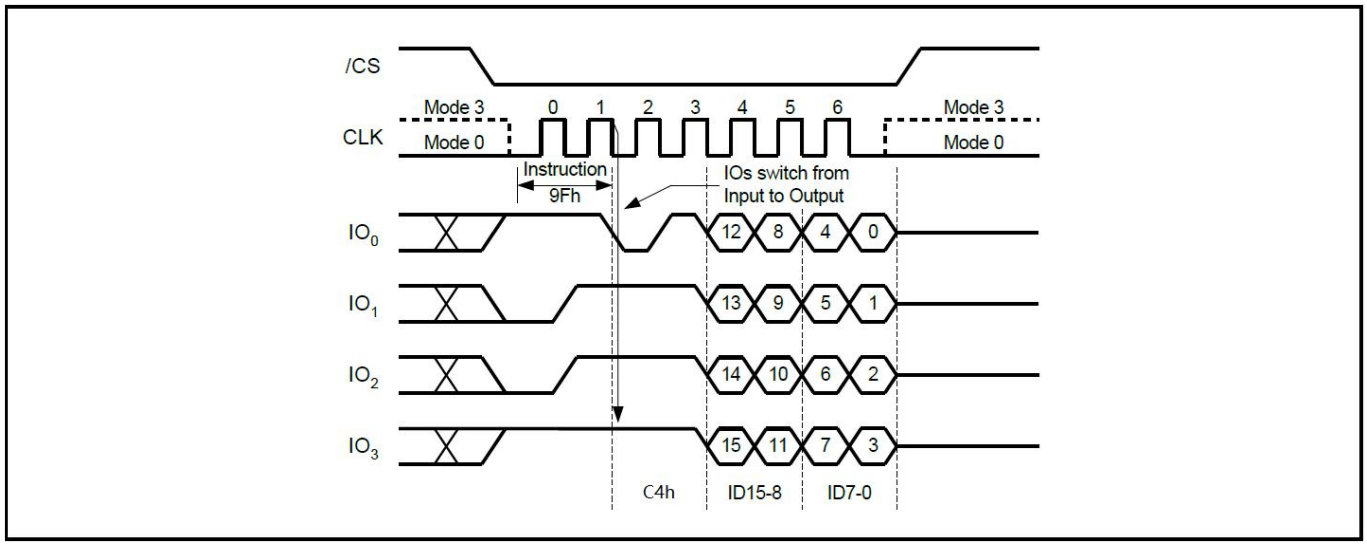


Figure 26b.Read Identification ID Sequence Diagram for QPI Mode

9.30 Read Unique ID Number (4Bh)

The Read Unique ID Number instruction accesses a factory-set read-only 64-bit number that is unique to each GT25Q16BL device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID instruction is initiated by driving the /CS pin low and shifting the instruction code "4Bh" followed by a four bytes of dummy clocks. After which, the 64- bit ID is shifted out on the falling edge of CLK as shown in figure 27.

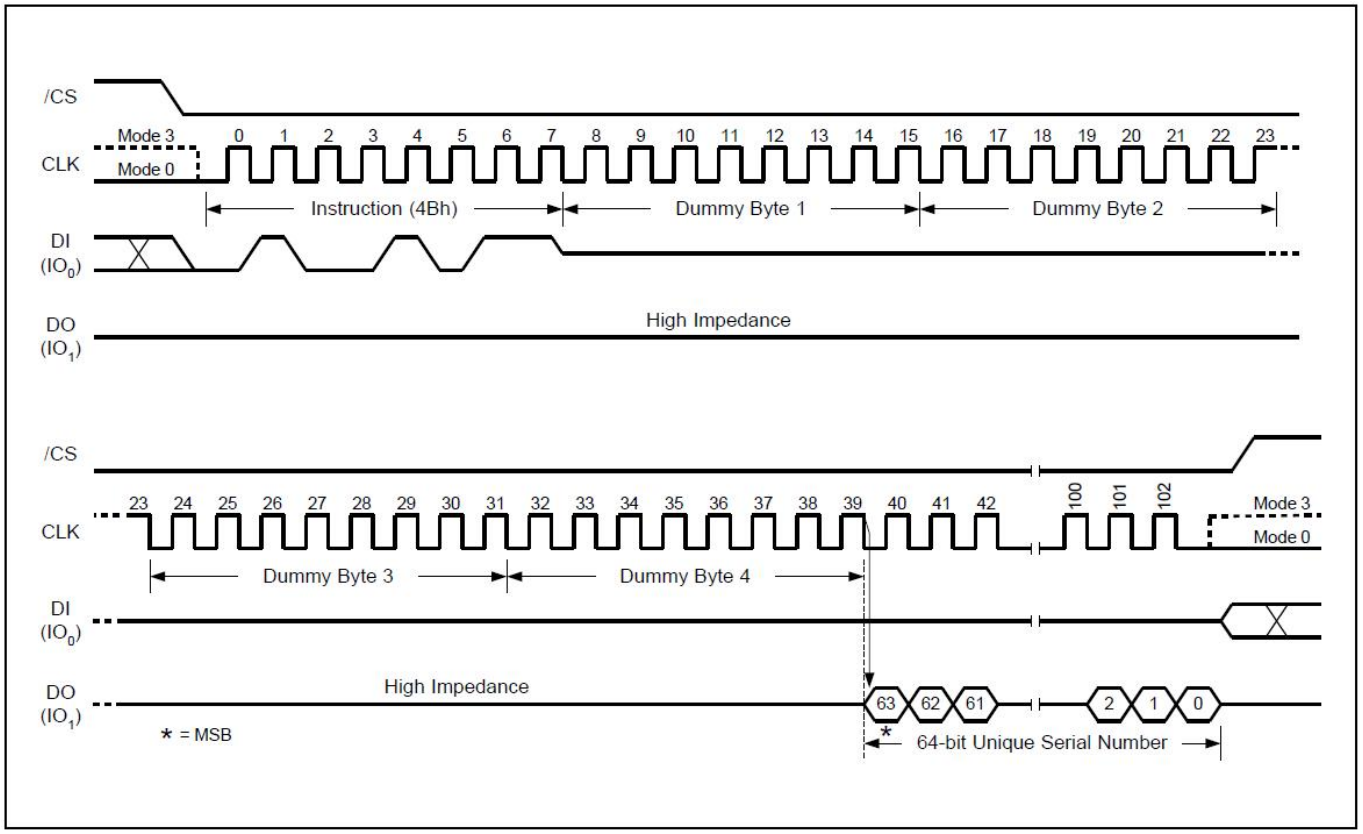


Figure 27. Read Unique ID Number Instruction Sequence

9.31 Program/Erase Suspend (PES) (75H)

The Erase/Program Suspend instruction “75h”, allows the system to interrupt a Sector or Block Erase operation or a Page Program operation and then read from or program/erase data to, any other sectors or blocks. The Erase/Program Suspend instruction sequence is shown in Figure 28a & 28b.

The Write Status Register instruction (01h) and Erase instructions (20h, 52h, D8h, C7h, 60h, 44h) are not allowed during Erase Suspend. Erase Suspend is valid only during the Sector or Block erase operation. If written during the Chip Erase operation, the Erase Suspend instruction is ignored. The Write Status Register instruction (01h) and Program instructions (02h, 32h, 42h) are not allowed during Program Suspend. Program Suspend is valid only during the Page Program or Quad Page Program operation.

The Erase/Program Suspend instruction “75h” will be accepted by the device only if the SUS bit in the Status Register equals to 0 and the BUSY bit equals to 1 while a Sector or Block Erase or a Page Program operation is on-going. If the SUS bit equals to 1 or the BUSY bit equals to 0, the Suspend instruction will be ignored by the device. A maximum of time of “tSUS” (See AC Characteristics) is required to suspend the erase or program operation. The BUSY bit in the Status Register will be cleared from 1 to 0 within “tSUS” and the SUS bit in the Status Register will be set from 0 to 1 immediately after Erase/Program Suspend. For a previously resumed Erase/Program operation, it is also required that the Suspend instruction “75h” is not issued earlier than a minimum of time of “tSUS” following the preceding Resume instruction “7Ah”.

Unexpected power off during the Erase/Program suspend state will reset the device and release the suspend state. SUS bit in the Status Register will also reset to 0. The data within the page, sector or block that was being suspended may become corrupted. It is recommended for the user to implement system design techniques against the accidental power interruption and preserve data integrity duringerase/program suspend state.

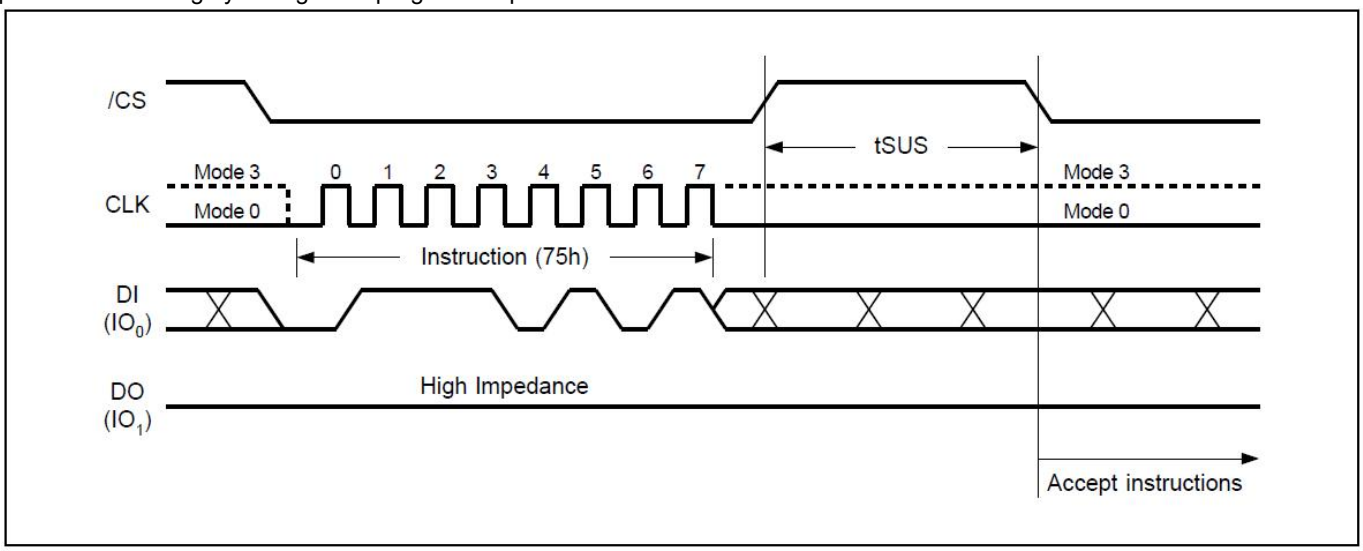


Figure 28a. Program/Erase Suspend Sequence Diagram for SPI Mode

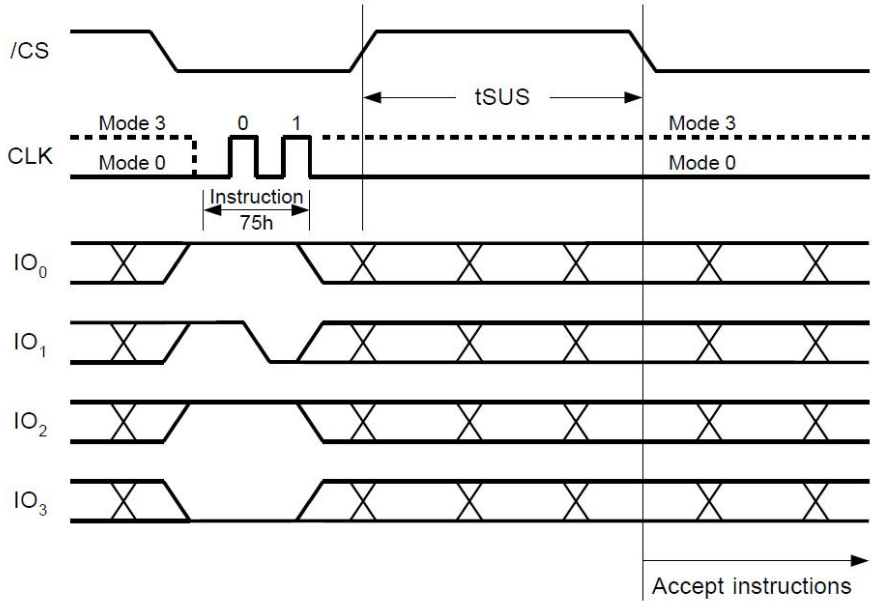


Figure 28b. Program/Erase Suspend Sequence Diagram for QPI Mode

9.32 Program/Erase Resume (PER) (7AH)

The Erase/Program Resume instruction “7Ah” must be written to resume the Sector or Block Erase operation or the Page Program operation after an Erase/Program Suspend. The Resume instruction “7Ah” will be accepted by the device only if the SUS bit in the Status Register equals to 1 and the BUSY bit equals to 0. After issued the SUS bit will be cleared from 1 to 0 immediately, the BUSY bit will be set from 0 to 1 within 200ns and the Sector or Block will complete the erase operation or the page will complete the program operation. If the SUS bit equals to 0 or the BUSY bit equals to 1, the Resume instruction “7Ah” will be ignored by the device. The Erase/Program Resume instruction sequence is shown in Figure 29.

Resume instruction is ignored if the previous Erase/Program Suspend operation was interrupted by unexpected power off. It is also required that a subsequent Erase/Program Suspend instruction not to be issued within a minimum of time of “tSUS” following a previous Resume instruction.

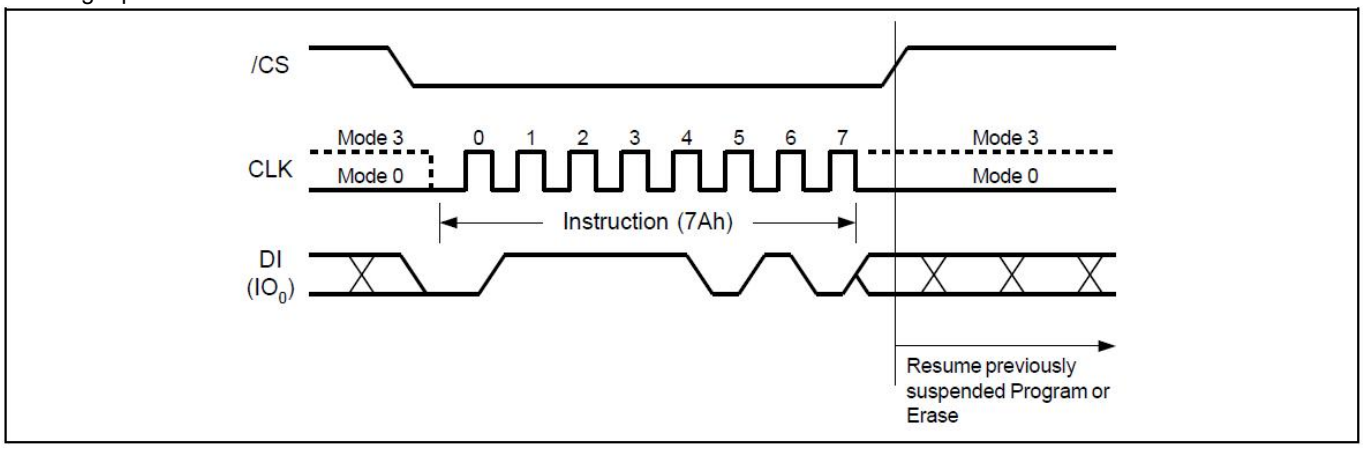


Figure 29a. Program/Erase Resume Sequence Diagram for SPI Mode

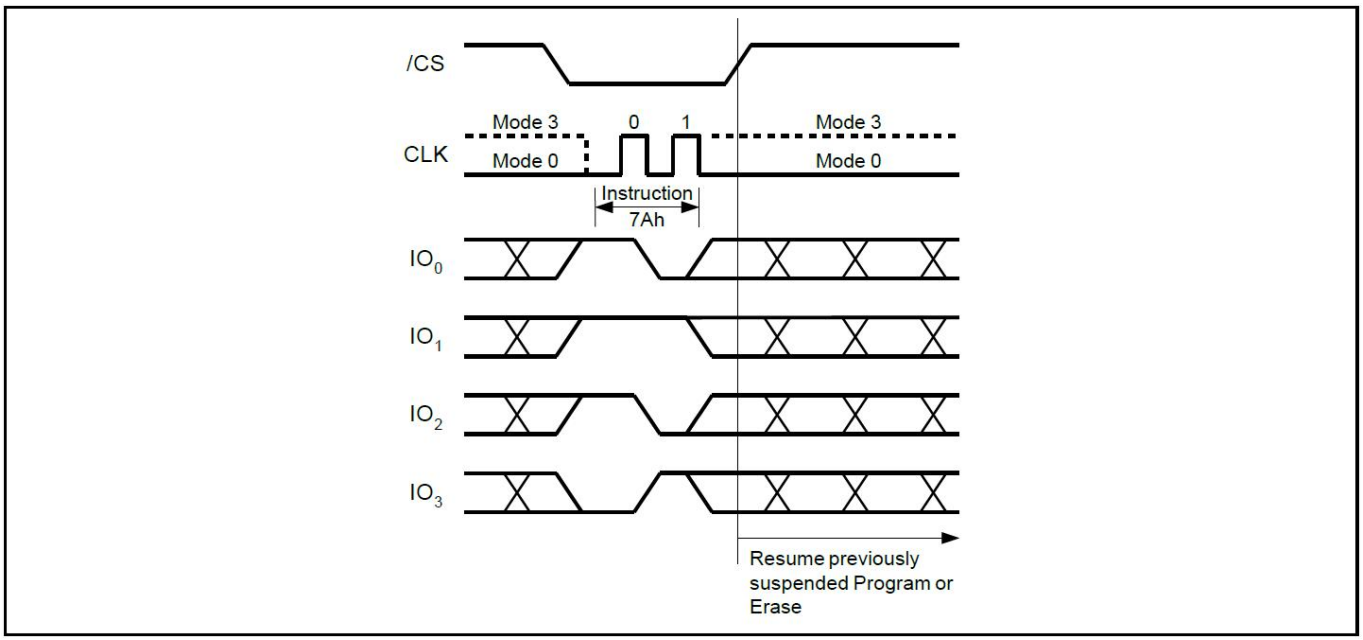


Figure 29b. Program/Erase Resume Sequence Diagram for QPI Mode

9.33 Enable Reset (66H) and Reset (99H)

If the Reset command is accepted, any on-going internal operation will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch status (WEL), Program/Erase Suspend status, Read Parameter setting (P7-P0), Deep Power Down Mode, Continuous Read Mode bit setting (M7-M0) and Wrap Bit Setting (W6-W4).

The "Enable Reset (66H)" and the "Reset (99H)" commands can be issued in either SPI mode. The "Reset (99H)" command sequence as follow: CS# goes low → Sending Enable Reset command → CS# goes high → CS# goes low → Sending Reset command → CS# goes high. Once the Reset command is accepted by the device, the device will take approximately tRST/tRST_E to reset. During this period, no command will be accepted. Data corruption may happen if there is an on-going or suspended internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the BUSY bit and the SUS bit in Status Register before issuing the Reset command sequence.

Data corruption may happen if there is an on-going or suspended internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the BUSY bit and the SUS bit in Status Register before issuing the Reset command sequence.

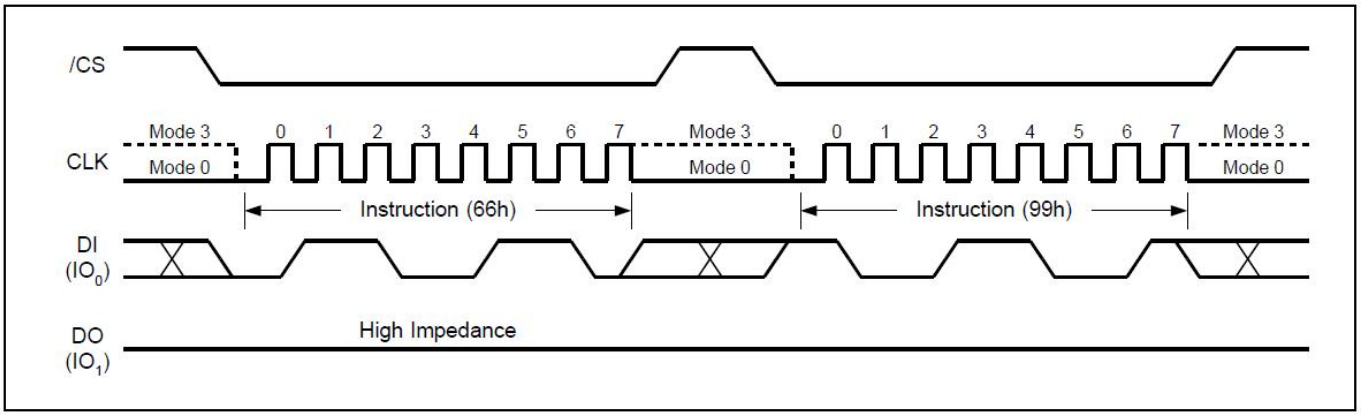


Figure 30a. Enable Reset and Reset Instruction Sequence for SPI Mode

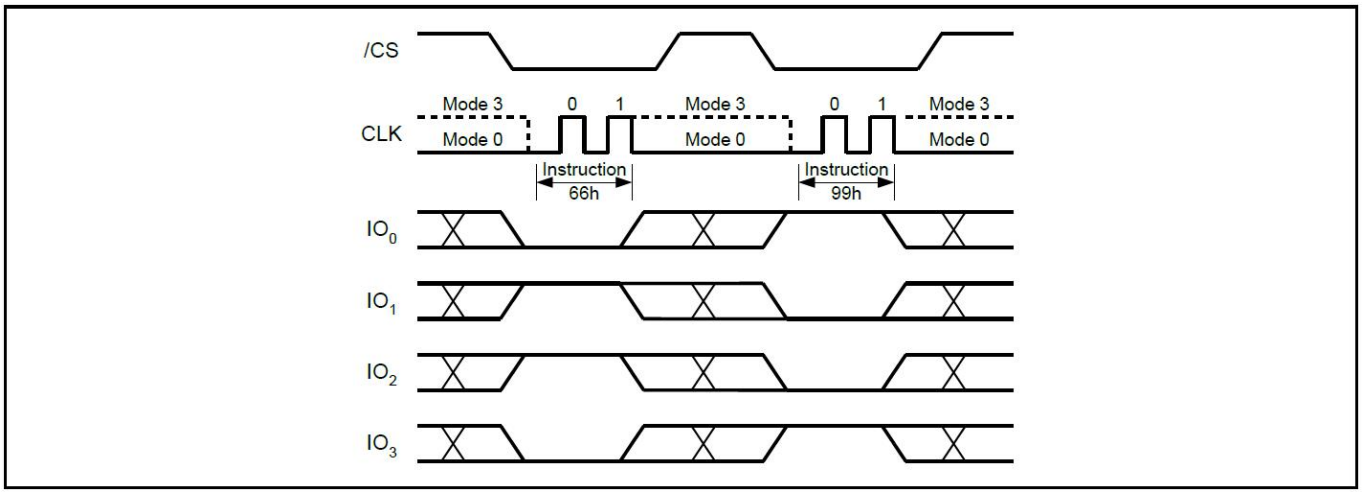


Figure 30b. Enable Reset and Reset Instruction Sequence for QPI Mode

9.34 Read SFDP Register (5Ah)

The GT25Q16BL features a 256-Byte Serial Flash Discoverable Parameter (SFDP) register that contains information about device configurations, available instructions and other features. The SFDP parameters are stored in one or more Parameter Identification (PID) tables. Currently only one PID table is specified, but more may be added in the future. The Read SFDP Register instruction is compatible with the SFDP standard initially established in 2010 for PC and other applications, as well as the JEDEC standard JESD216 that is published in 2011. Most Giantec SpiFlash Memories shipped after June 2011 (date code 1124 and beyond) support the SFDP feature as specified in the applicable datasheet.

The Read SFDP instruction is initiated by driving the /CS pin low and shifting the instruction code "5Ah"followed by a 24-bit address (A23-A0)(1) into the DI pin. Eight "dummy" clocks are also required before the SFDP register contents are shifted out on the falling edge of the 40th CLK with most significant bit (MSB) first as shown in Figure 31. For SFDP register values and descriptions, please refer to the Giantec Application Note for SFDP Definition Table.

Note: 1. A23-A8 = 0; A7-A0 are used to define the starting byte address for the 256-Byte SFDP Register.

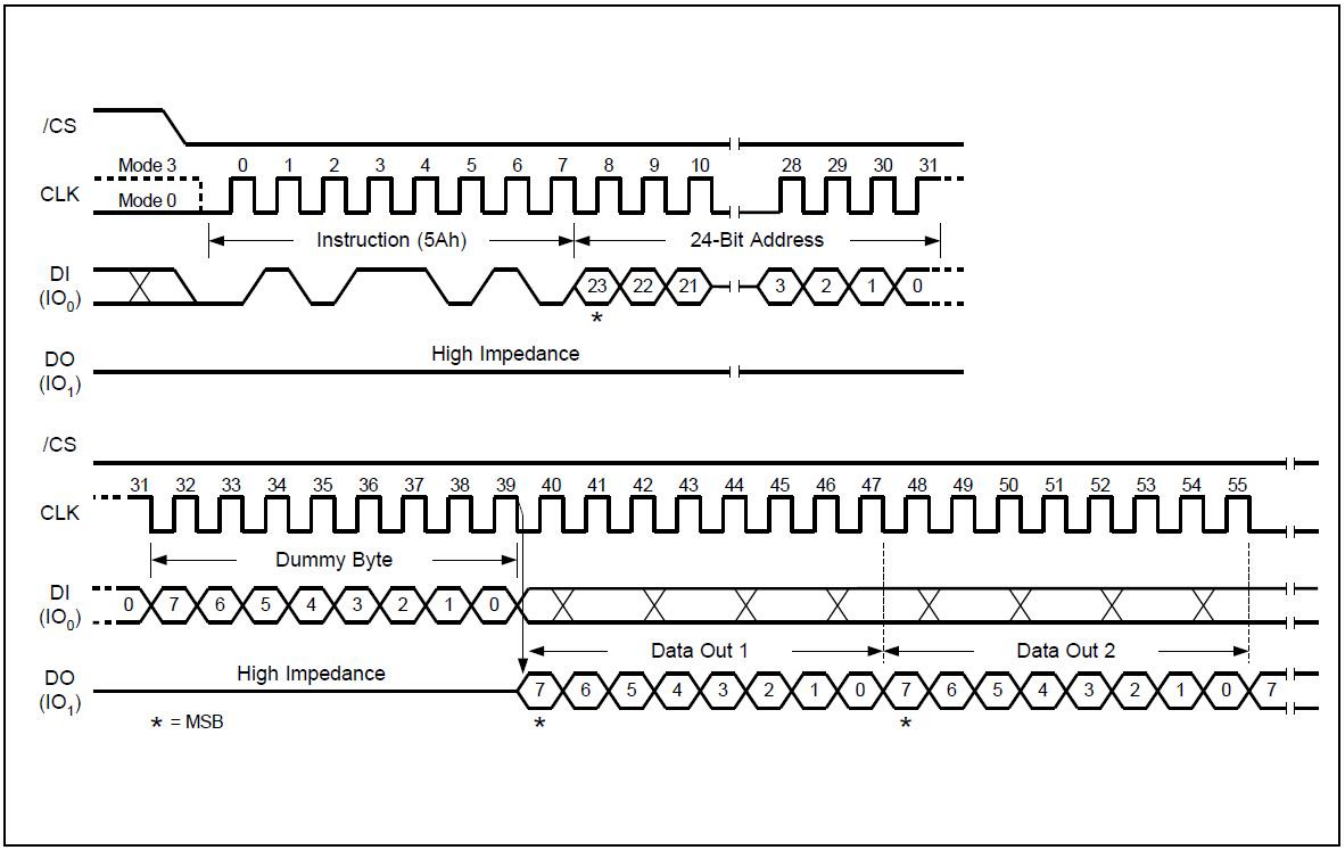


Figure 31. Read SFDP Register Instruction Sequence Diagram(SPI mode only)

Signature and Parameter Identification Data Values

Description	Comment	Byte Add(H)	Bit Add	Data	Data
SFDP Signature	Fixed:50444653H	00H	07:00	53H	53H
		01H	15:08	46H	46H
		02H	23:16	44H	44H
		02H	31:24	50H	50H
SFDP Minor Revision Number	Start from 00H	04H	07:00	00H	00H
SFDP Major Revision Number	Start from 01H	05H	15:08	01H	01H
Number of Parameters Headers	Start from 00H	06H	23:16	01H	01H
Unused	Contains 0xFFH and can never be changed	07H	31:24	FFH	FFH
ID number (JEDEC)	00H: It indicates a JEDEC specified header	08H	07:00	00H	00H
Parameter Table Minor Revision Number	Start from 0x00H	09H	15:08	00H	00H
Parameter Table Major Revision Number	Start from 0x01H	0AH	23:16	01H	01H
Parameter Table Length (in double word)	How many DWORDs in the Parameter table	0BH	31:24	09H	09H
Parameter Table Pointer (PTP)	First address of JEDEC Flash Parameter table	0CH	07:00	30H	30H
		0DH	15:08	00H	00H
		0EH	23:16	00H	00H
Unused	Contains 0xFFH and can never be changed	0FH	31:24	FFH	FFH
ID Number LSB (Giantec Manufacturer ID)	It is indicates Giantec manufacturer ID	10H	07:00	C4H	C4H
Parameter Table Minor Revision Number	Start from 0x00H	11H	15:08	00H	00H
Parameter Table Major Revision Number	Start from 0x01H	12H	23:16	01H	01H
Parameter Table Length (in double word)	How many DWORDs in the Parameter table	13H	31:24	03H	03H
Parameter Table Pointer (PTP)	First address of Giantec Flash Parameter table	14H	07:00	60H	60H
		15H	15:08	00H	00H
		16H	23:16	00H	00H
Unused	Contains 0xFFH and can never be changed	17H	31:24	FFH	FFH

Description	Comment	Byte Add(H)	Bit Add	Data	Data
Unuse	. . .	. . .	. . .	FFH	FFH
Block/Sector Erase Size	00: Reserved; 01: 4KB erase; 10: Reserved; 11: not support 4KB erase	30H	01:00	01b	E5H
Write Granularity	0: 1Byte, 1: 64Byte or larger		02	1b	
Write Enable Instruction Requested for Writing to Volatile Status Registers	0: Nonvolatile status bit 1: Volatile status bit (BP status register bit)		03	0b	
Write Enable Opcode Select for Writing to Volatile Status Registers	0: Use 50H Opcode, 1: Use 06H Opcode, Note: If target flash status register is Nonvolatile, then bits 3 and 4 must be set to 00b.		04	0b	
Unused	Contains 111b and can never be changed		07:05	111b	
4KB Erase Opcode		31H	15:08	20H	20H
(1-1-2) Fast Read	0=Not support, 1=Support	32H	16	1b	F1H
Address Bytes Number used in addressing flash array	00: 3Byte only, 01: 3 or 4Byte, 10: 4Byte only, 11: Reserved		18:17	00b	
Double Transfer Rate (DTR) clocking	0=Not support, 1=Support		19	0b	
(1-2-2) Fast Read	0=Not support, 1=Support		20	1b	
(1-4-4) Fast Read	0=Not support, 1=Support		21	1b	
(1-1-4) Fast Read	0=Not support, 1=Support		22	1b	
Unused			23	1b	
Unused		33H	31:24	FFH	FFH
Flash Memory Density		37H:34H	31:00	00FFFFFFH(16Mb)	
(1-4-4) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	38H	04:00	00100b	44H
(1-4-4) Fast Read Number of Mode Bits	000b:Mode Bits not support		07:05	010b	
(1-4-4) Fast Read Opcode		39H	15:08	EBH	EBH

Description	Comment	Byte Add(H)	Bit Add	Data	Data
(1-1-4) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	3AH	20:16	01000b	08H
(1-1-4) Fast Read Number of Mode Bits	000b:Mode Bits not support		23:21	000b	
(1-1-4) Fast Read Opcode		3BH	31:24	6BH	6BH
(1-1-2) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	3CH	04:00	01000b	08H
(1-1-2) Fast Read Number of Mode Bits	000b: Mode Bits not support		07:05	000b	
(1-1-2) Fast Read Opcode		3DH	15:08	3BH	3BH
(1-2-2) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	3EH	20:16	00010b	42H
(1-2-2) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	010b	
(1-2-2) Fast Read Opcode		3FH	31:24	BBH	BBH
(2-2-2) Fast Read	0=not support 1=support	40H	00	0b	FEH
Unused			03:01	111b	
(4-4-4) Fast Read	0=not support 1=support		04	1b	
Unused			07:05	111b	
Unused		43H:41H	31:08	0xFFH	0xFFH
Unused		45H:44H	15:00	0xFFH	0xFFH
(2-2-2) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	46H	20:16	00000b	00H
(2-2-2) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	000b	
(2-2-2) Fast Read Opcode		47H	31:24	FFH	FFH
Unused		49H:48H	15:00	0xFFH	0xFFH
(4-4-4) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	4AH	20:16	00000b	00H
(4-4-4) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	000b	
(4-4-4) Fast Read Opcode		4BH	31:24	FFH	FFH
Sector Type 1 Size	Sector/block size=2^N bytes 0x00b: this sector type don't exist	4CH	07:00	0CH	0CH
Sector Type 1 erase Opcode		4DH	15:08	20H	20H
Sector Type 2 Size	Sector/block size=2^N bytes 0x00b: this sector type don't exist	4EH	23:16	0FH	0FH

Description	Comment	Byte Add(H)	Bit Add	Data	Data
Sector Type 2 erase Opcode		4FH	31:24	52H	52H
Sector Type 3 Size	Sector/block size=2^N bytes 0x00b: this sector type don't exist	50H	07:00	10H	10H
Sector Type 3 erase Opcode		51H	15:08	D8H	D8H
Sector Type 4 Size	Sector/block size=2^N bytes 0x00b: this sector type don't exist	52H	23:16	00H	00H
Sector Type 4 erase Opcode		53H	31:24	FFH	FFH
Unused	. . .	. . .	. . .	FFH	FFH
Vcc Supply Maximum Voltage	1950H=1.950V	61H:60H	15:00	3600H	3600H
	2000H=2.000V				
	2100H=2.100V				
	2700H=2.700V				
	3600H=3.600V				
Vcc Supply Minimum Voltage	1650H=1.650V	63H:62H	31:16	1650H	1650H
	2250H=2.250V				
	2350H=2.350V				
	2700H=2.700V				
HW Reset# pin	0=not support 1=support	65H:64H	00	0b	F99EH
HW Hold# pin	0=not support 1=support		01	1b	
Deep Power Down Mode	0=not support 1=support		02	1b	
SW Reset	0=not support 1=support		03	1b	
SW Reset Opcode	Should be issue Reset Enable(66H) before Reset cmd.		11:04	99H	
Program Suspend/Resume	0=not support 1=support		12	1b	
Erase Suspend/Resume	0=not support 1=support		13	1b	
Unused			14	1b	
Wrap-Around Read mode	0=not support 1=support		15	1b	
Wrap-Around Read mode Opcode		66H	23:16	77H	77H
Wrap-Around Read data length	08H:support 8B wrap-around read 16H:8B&16B 32H:8B&16B&32B 64H:8B&16B&32B&64B	67H	31:24	64H	64H

Description	Comment	Byte Add(H)	Bit Add	Data	Data
Individual block lock	0=not support 1=support	6BH:68 H	00	0b	CBFCH
Individual block lock bit (Volatile/Nonvolatile)	0=Volatile 1=Nonvolatile		01	0b	
Individual block lock Opcode			09:02	FFH	
Individual block lock Volatile protect bit default protect status	0=protect 1=unprotect		10	0b	
Secured OTP	0=not support 1=support		11	1b	
Read Lock	0=not support 1=support		12	0b	
Permanent Lock	0=not support 1=support		13	0b	
Unused			15:14	11b	
Unused			31:16	FFFFH	FFFFH
Unused	. . .	. . .	. . .	FFH	FFH
Unused		FFH	FFH	FFH	FFH

9.34 Erase Security Registers (44h)

The GT25Q16BL offers Four 256-byte Security Registers which can be erased and programmed individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Register instruction is similar to the Sector Erase instruction. A Write Enable instruction must be executed before the device will accept the Erase Security Register Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code "44h" followed by a 24-bit address (A23-A0) to erase all four security registers.

ADDRESS	A23-A16	A15-A8	A7-A0
Security Register #1,#2,#3,#4	00h	00H	Don't Care

The Erase Security Register instruction sequence is shown in Figure 32. The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the instruction will not be executed. After /CS is driven high, the self-timed Erase Security Register operation will commence for a time duration of tSE (See AC Characteristics). While the Erase Security Register cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Erase Security Register cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Security Register Lock Bits LB in the Status Register-2 can be used to OTP protect the security registers. Once a lock bit is set to 1, the corresponding security register will be permanently locked, Erase Security Register instruction to that register will be ignored.

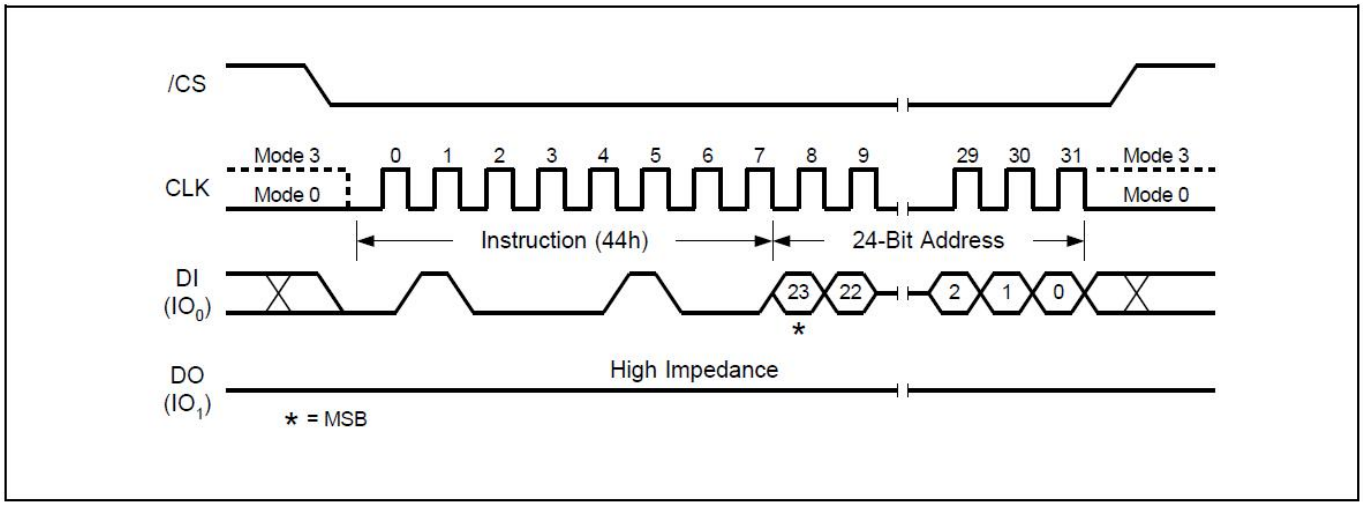


Figure 32. Erase Security Registers Instruction (SPI Mode only)

9.35 Program Security Registers (42h)

The Program Security Register instruction is similar to the Page Program instruction. It allows from one byte to 256 bytes of security register data to be programmed at previously erased (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Program Security Register Instruction (Status Register bit WEL= 1). The instruction is initiated by driving the /CS pin low then shifting the instruction code "42h" followed by a 24-bit address (A23-A0) and at least one data byte, into the DI pin. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device.

ADDRESS	A23-A16	A15-A8	A7-A0
Security Register #1	00h	00H	Byte Address
Security Register #2	00h	01H	Byte Address
Security Register #3	00h	02H	Byte Address
Security Register #4	00h	03H	Byte Address

The Program Security Register instruction sequence is shown in Figure 33. The Security Register Lock Bits LB in the Status Register-2 can be used to OTP protect the security registers. Once a lock bit is set to 1, the corresponding security register will be permanently locked, Program Security Register instruction to that register will be ignored

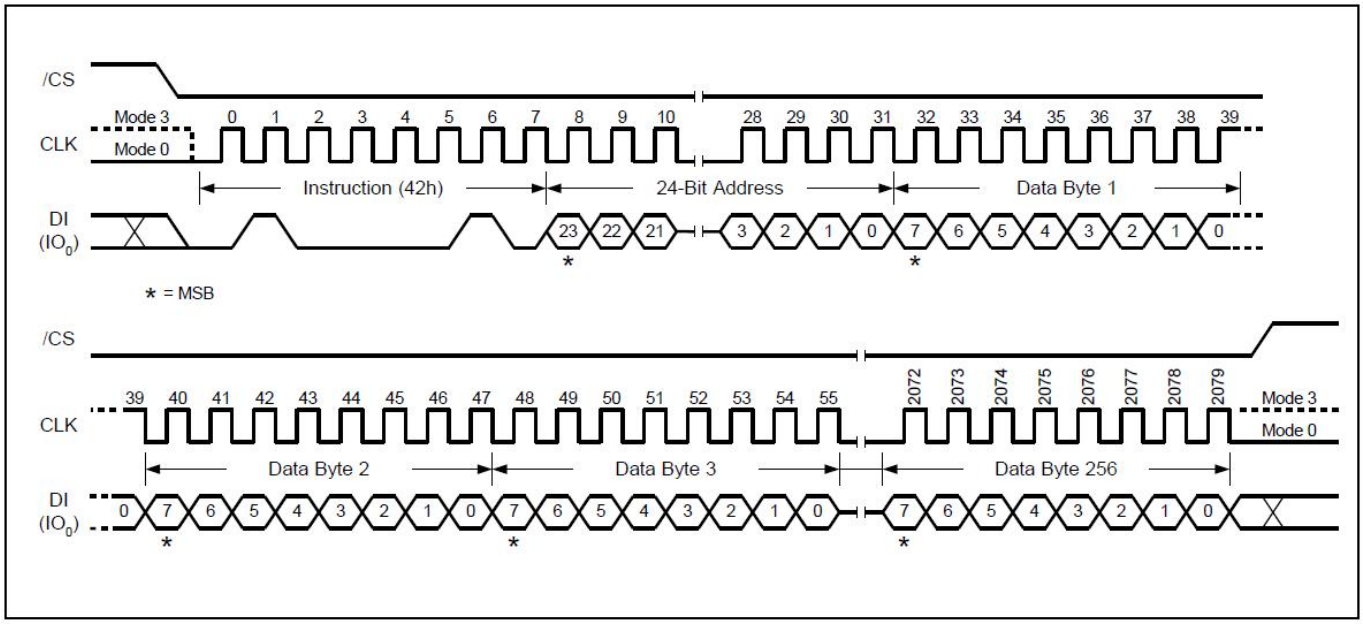


Figure 33. Program Security Registers Instruction (SPI Mode only)

9.36 Read Security Registers (48h)

The Read Security Register instruction is similar to the Fast Read instruction and allows one or more data bytes to be sequentially read from one of the three security registers. The instruction is initiated by driving the /CS pin low and then shifting the instruction code "48h" followed by a 24-bit address (A23-A0) and eight "dummy" clocks into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The byte address is automatically incremented to the next byte address after each byte of data is shifted out. Once the byte address reaches the last byte of the register (byte FFh), it will reset to 00h, the first byte of the register, and continue to increment. The instruction is completed by driving /CS high. The Read Security Register instruction sequence is shown in Figure 34. If a Read Security Register instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle. The Read Security Register instruction allows clock rates from D.C. to a maximum of FR (see AC Electrical Characteristics).

ADDRESS	A23-A16	A15-A8	A7-A0
Security Register #1	00h	00H	Byte Address
Security Register #2	00h	01H	Byte Address
Security Register #3	00h	02H	Byte Address
Security Register #4	00h	03H	Byte Address

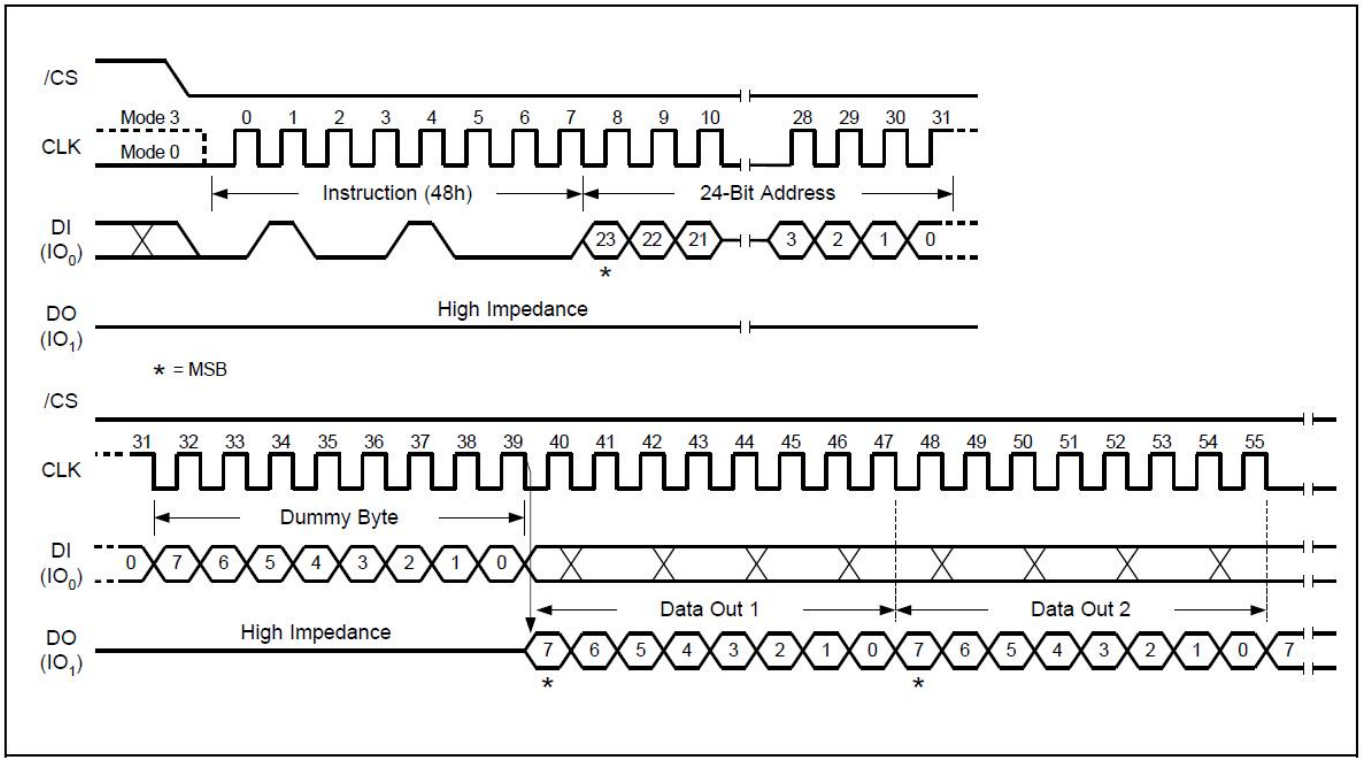


Figure 34. Read Security Registers Instruction (SPI Mode only)

9.37 Set Read Parameters (C0h)

In QPI mode, to accommodate a wide range of applications with different needs for either maximum read frequency or minimum data access latency, "Set Read Parameters (C0h)" instruction can be used to configure the number of dummy clocks for "Fast Read (0Bh)", "Fast Read Quad I/O (EBh)" & "Burst Read with Wrap (0Ch)" instructions, and to configure the number of bytes of "Wrap Length" for the "Burst Read with Wrap (0Ch)" instruction.

In Standard SPI mode, the "Set Read Parameters (C0h)" instruction is not accepted. The dummy clocks for various Fast Read instructions in Standard/Dual/Quad SPI mode are fixed, please refer to the Instruction Table 1-2 for details. The "Wrap Length" is set by W5-4 bit in the "Set Burst with Wrap (77h)" instruction. This setting will remain unchanged when the device is switched from Standard SPI mode to QPI mode.

The default "Wrap Length" after a power up or a Reset instruction is 8 bytes, the default number of dummy clocks is 2. The number of dummy clocks is only programmable for "Fast Read (0Bh)", "Fast Read Quad I/O (EBh)" & "Burst Read with Wrap (0Ch)" instructions in the QPI mode. Whenever the device is switched from SPI mode to QPI mode, the number of dummy clocks should be set again, prior to any 0Bh, EBh or 0Ch instructions.

P5 - P4	Dmmy Clock	Maximum Read FREQ
0 0	2	50MHz
0 1	4	60MHz
1 0	6	80MHz
1 1	8	104MHz

P1 - P0	Wrap Length
0 0	8-Byte
0 1	16-Byte
1 0	32-Byte
1 1	64-Byte

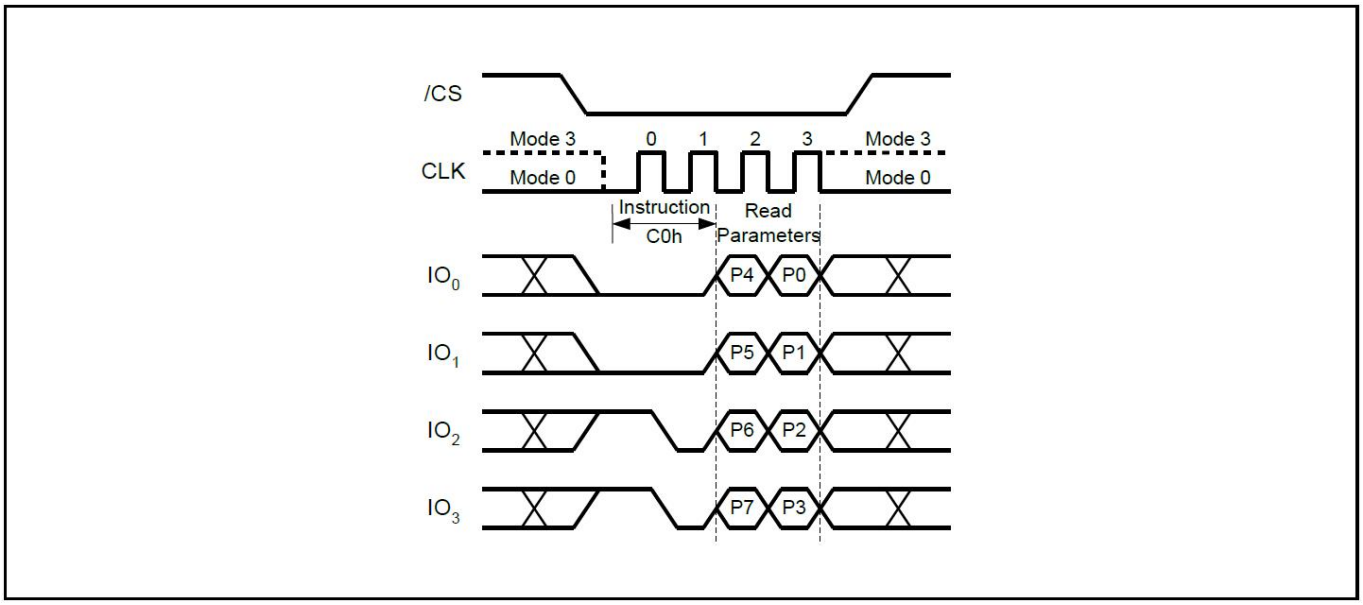


Figure 35. Set Read Parameters Instruction (QPI Mode only)

9.38 Burst Read with Wrap (0Ch)

The “Burst Read with Wrap (0Ch)” instruction provides an alternative way to perform the read operation with “Wrap Around” in QPI mode. The instruction is similar to the “Fast Read (0Bh)” instruction in QPI mode, except the addressing of the read operation will “Wrap Around” to the beginning boundary of the “Wrap Length” once the ending boundary is reached.

The “Wrap Length” and the number of dummy clocks can be configured by the “Set Read Parameters (C0h)” instruction.

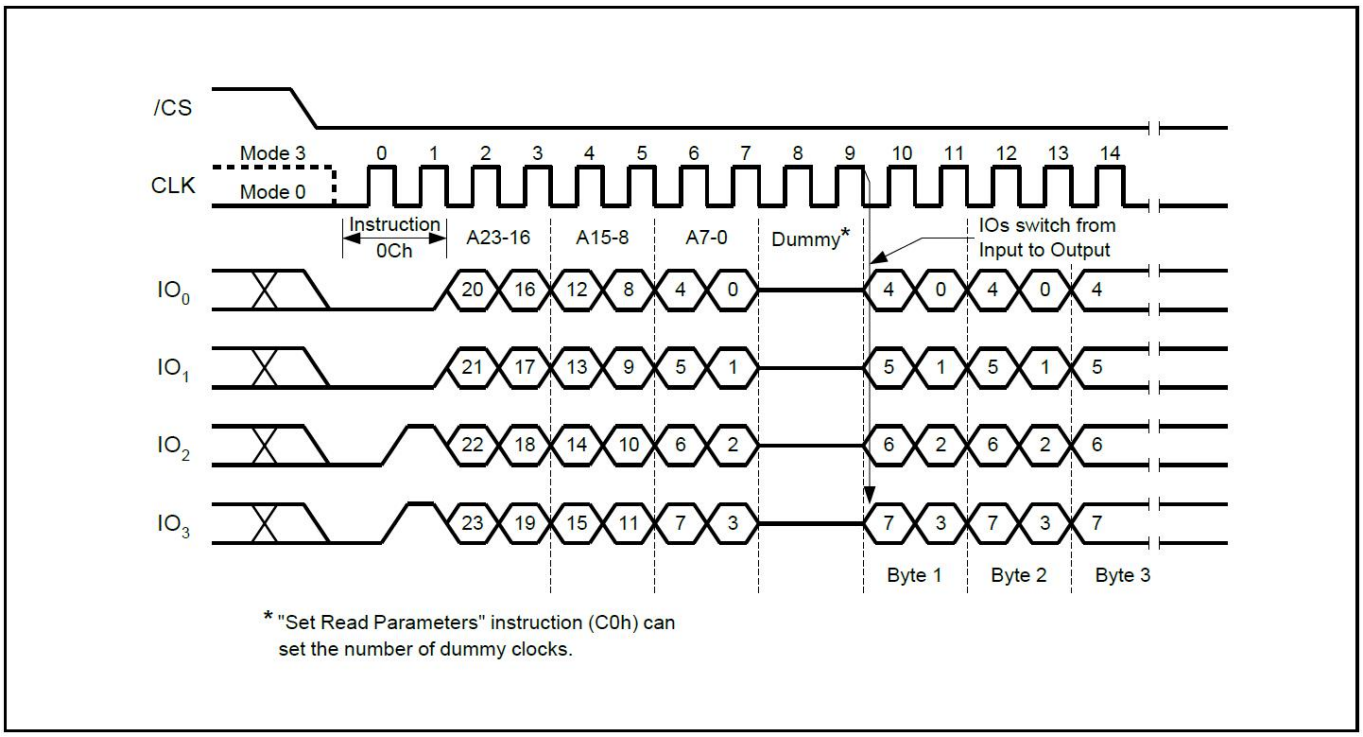


Figure 36. Burst Read with Wrap Instruction (QPI Mode only)

9.39 DTR Burst Read with Wrap (0Eh)

The "DTR Burst Read with Wrap (0Eh)" instruction provides an alternative way to perform the read operation with "Wrap Around" in QPI mode. The instruction is similar to the "Fast Read (0Bh)" instruction in QPI mode, except the addressing of the read operation will "Wrap Around" to the beginning boundary of the "Wrap Length" once the ending boundary is reached. The "Wrap Length" can be configured by the "Set Read Parameters (C0h)" instruction.

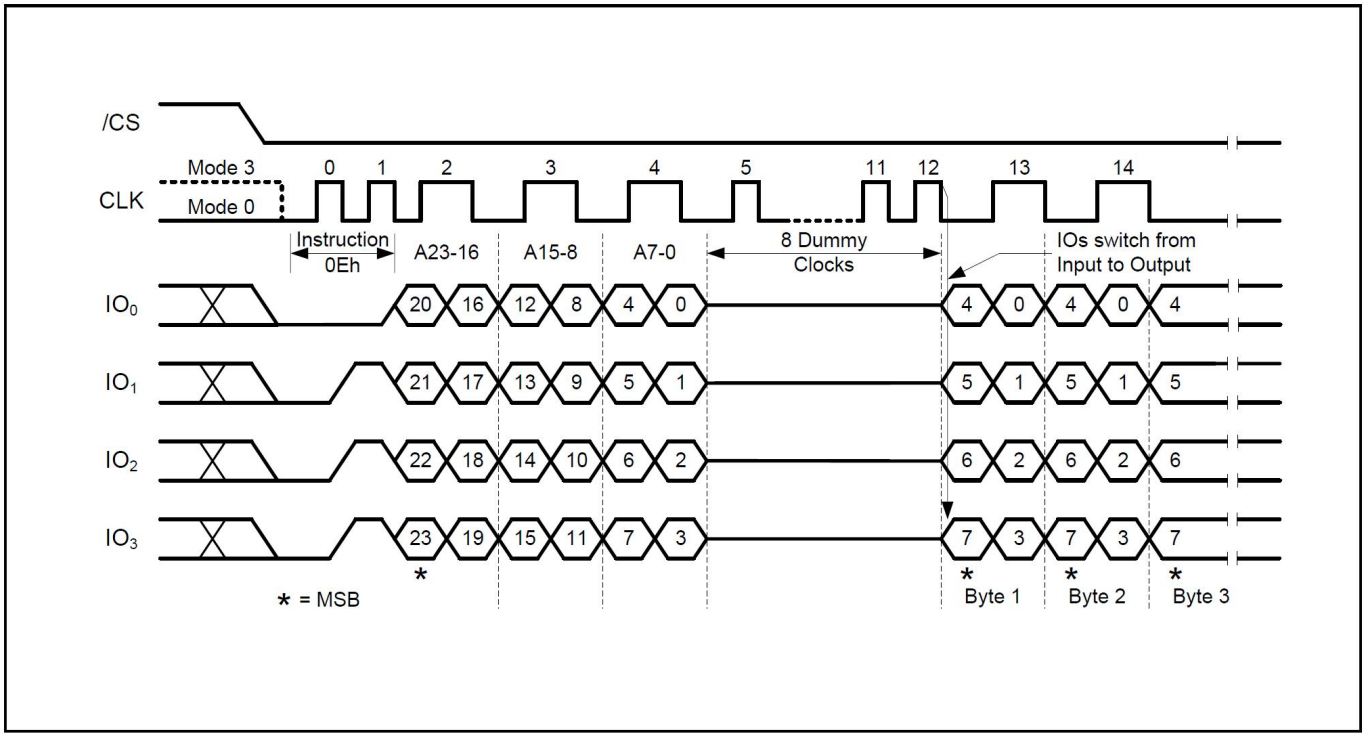


Figure 37. DTR Burst Read with Wrap Instruction (QPI Mode only)

9.40 Enter QPI Mode (38h)

The GT25Q16BL support both Standard/Dual/Quad Serial Peripheral Interface (SPI) and Quad Peripheral Interface (QPI). However, SPI mode and QPI mode cannot be used at the same time. “Enter QPI (38h)” instruction is the only way to switch the device from SPI mode to QPI mode.

Upon power-up, the default state of the device upon is Standard/Dual/Quad SPI mode. This provides full backward compatibility with earlier generations of Giantec serial flash memories. See Instruction Set Table 1-3 for all supported SPI commands. In order to switch the device to QPI mode, the Quad Enable (QE) bit in Status Register-2 must be set to 1 first, and an “Enter QPI (38h)” instruction must be issued. If the Quad Enable (QE) bit is 0, the “Enter QPI (38h)” instruction will be ignored and the device will remain in SPI mode.

See Instruction Set Table 3 for all the commands supported in QPI mode.
When the device is switched from SPI mode to QPI mode, the existing Write Enable and Program/Erase Suspend status, and the Wrap Length setting will remain unchanged.

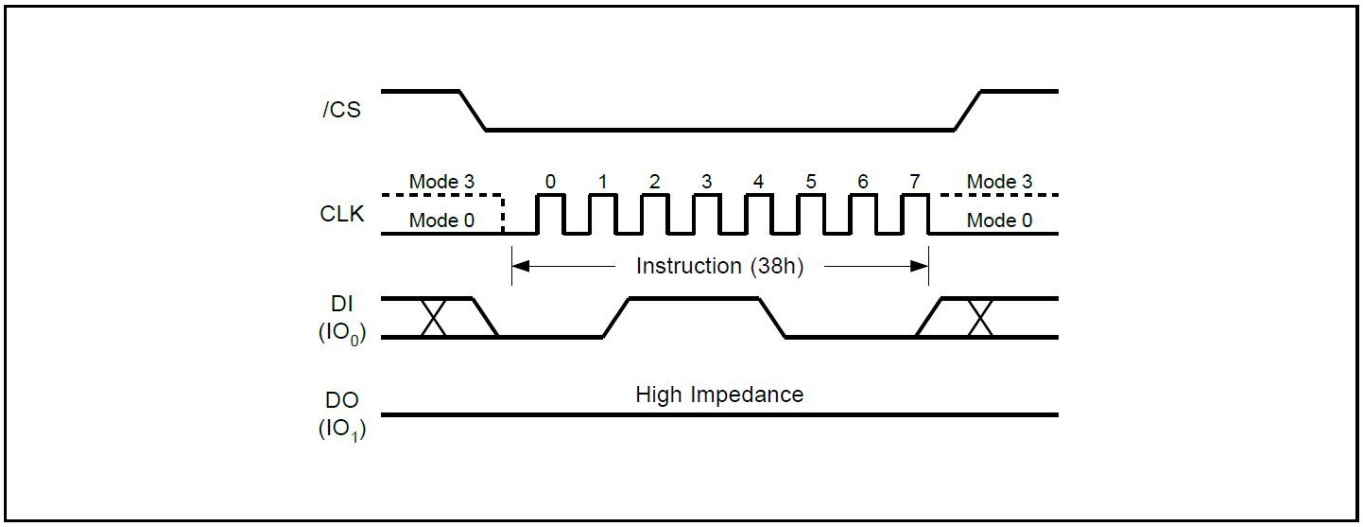


Figure 38. Enter QPI Instruction (SPI Mode only)

9.41 Exit QPI Mode (FFh)

In order to exit the QPI mode and return to the Standard/Dual/Quad SPI mode, an “Exit QPI (FFh)” instruction must be issued.

When the device is switched from QPI mode to SPI mode, the existing Write Enable Latch (WEL) and Program/Erase Suspend status, and the Wrap Length setting will remain unchanged.

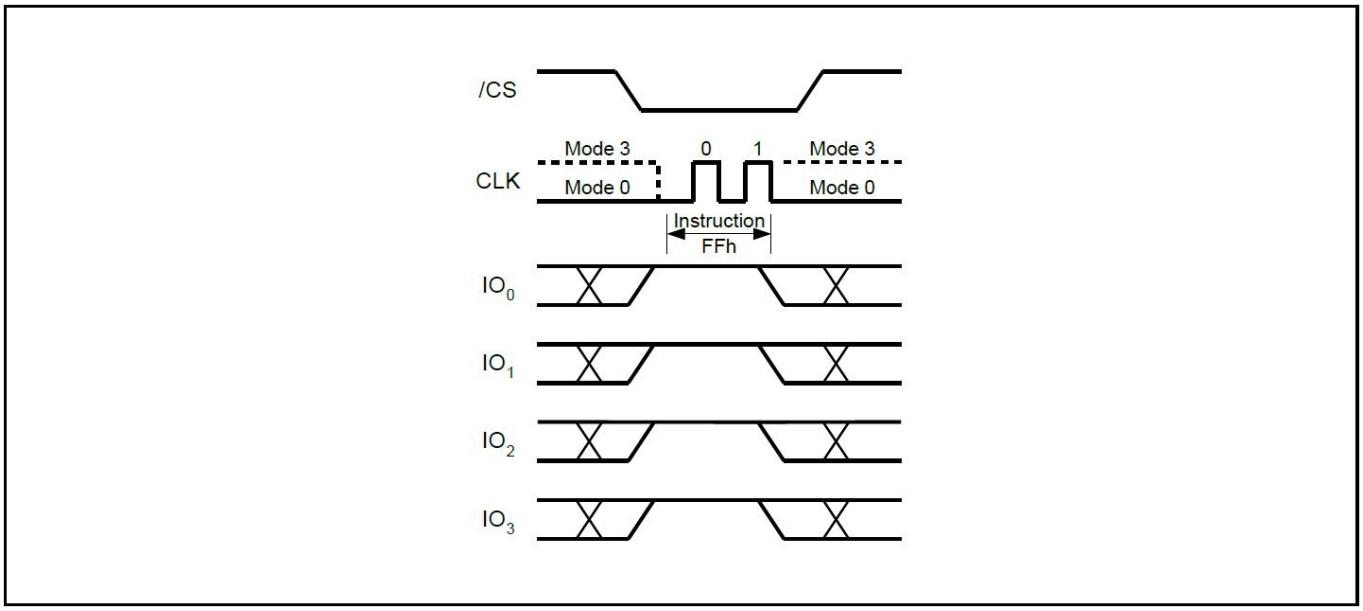
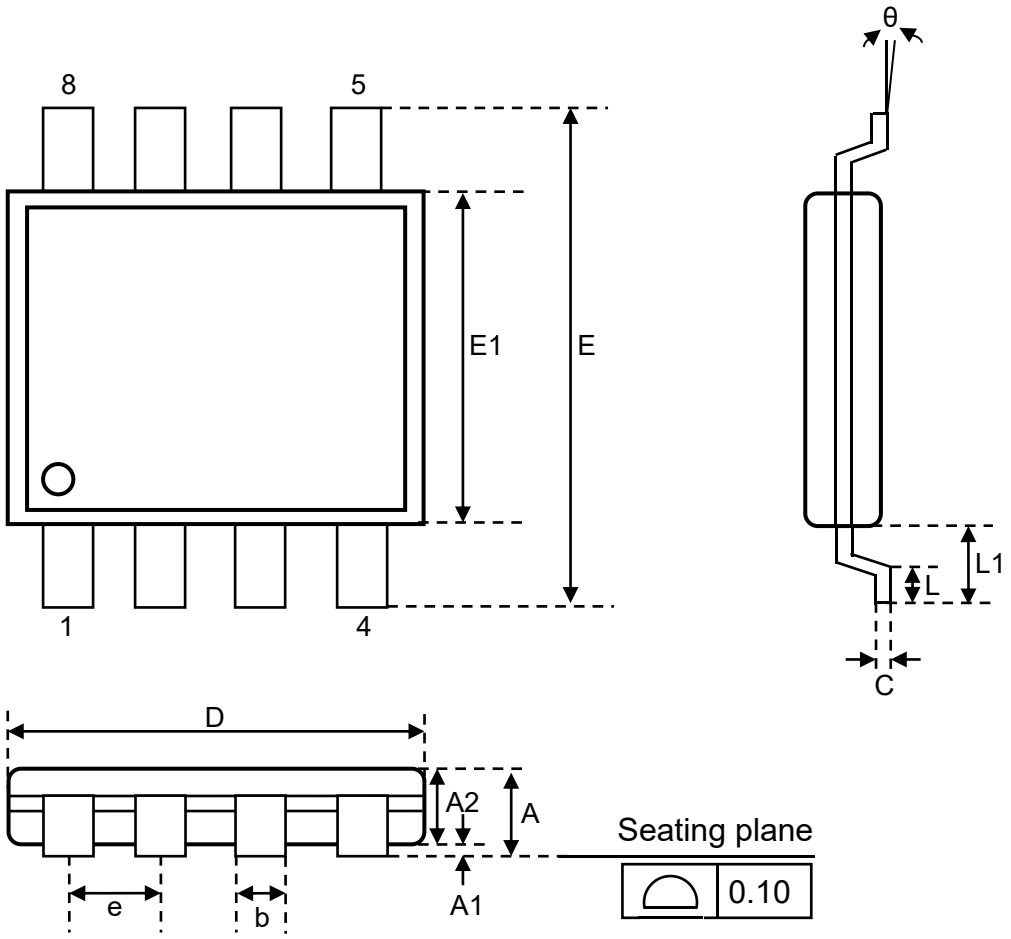


Figure 39 Exit QPI Instruction (QPI Mode only)

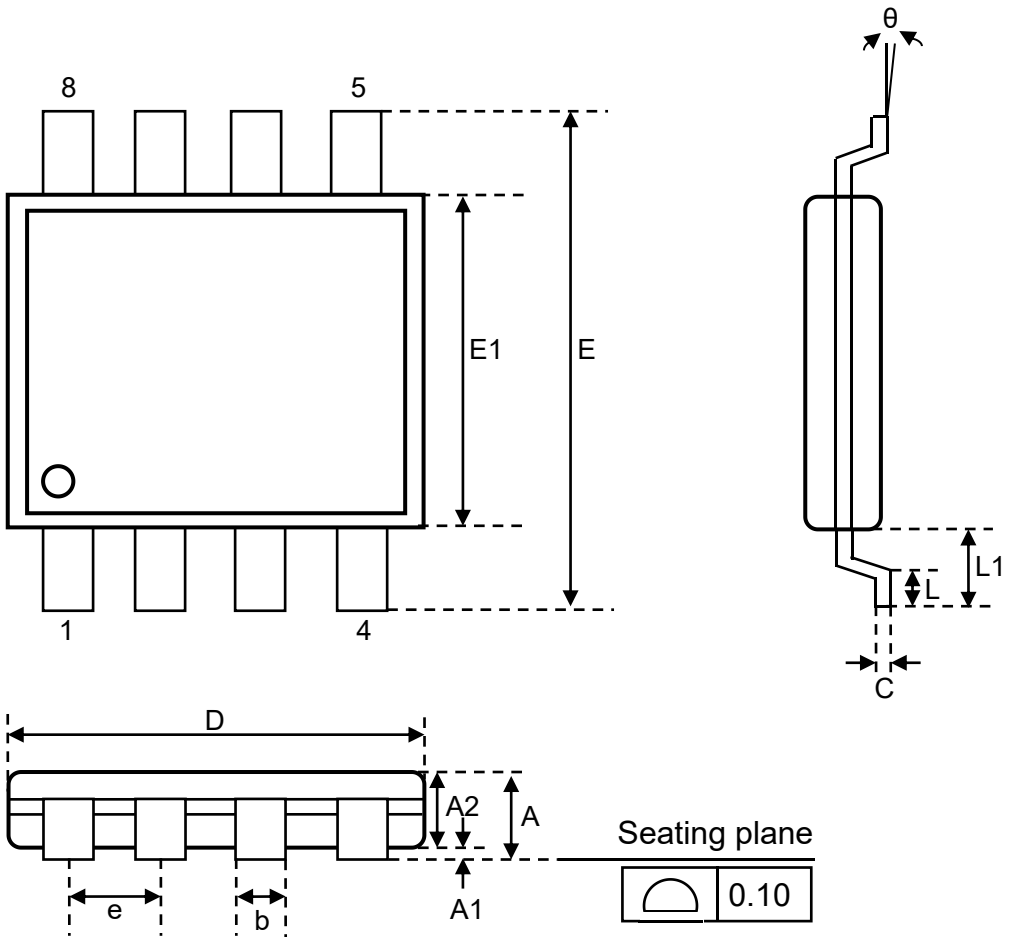
10 Package Information

10.1 Package SOP8 208MIL



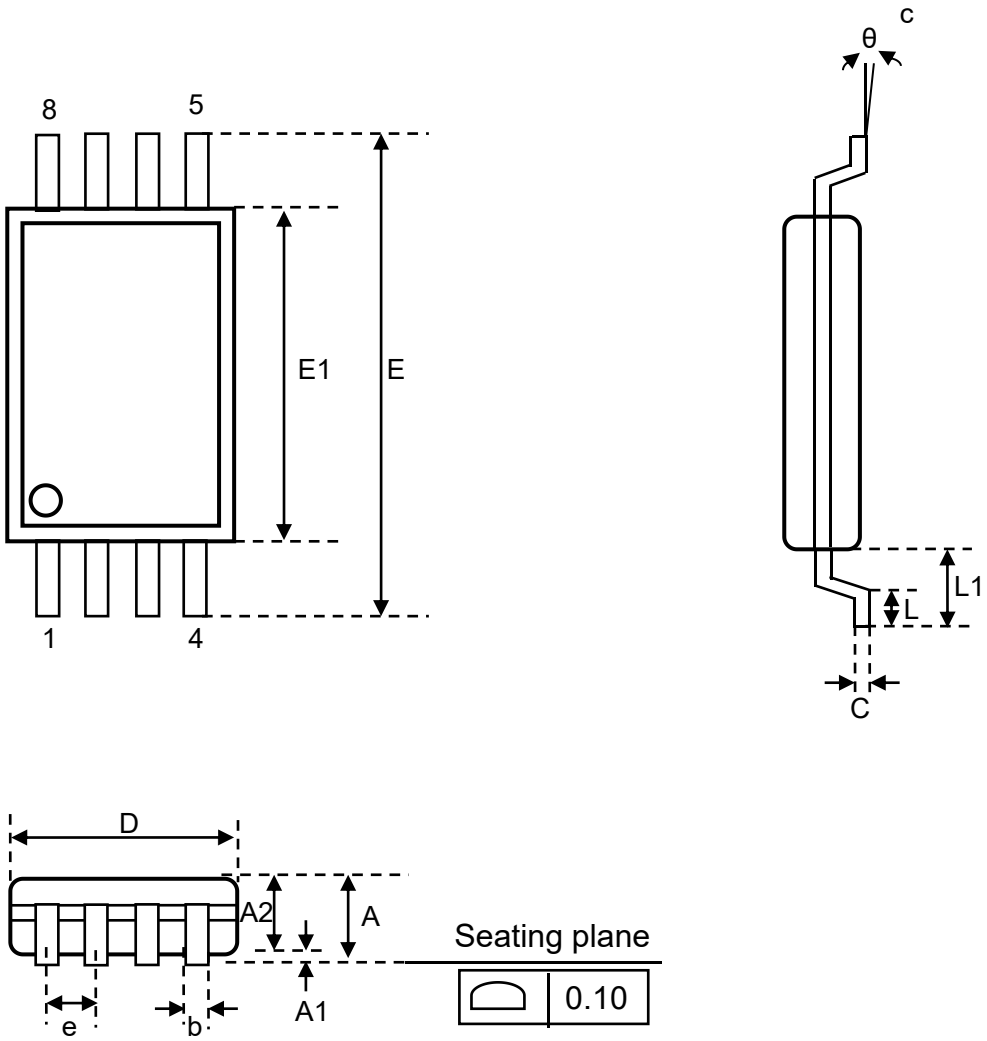
Symbol	mm			Inch		
	Min	Nom	Max	Min	Nom	Max
A	1.75	1.95	2.16	0.069	0.077	0.085
A1	0.05	0.15	0.25	0.002	0.006	0.010
A2	1.70	1.80	1.91	0.067	0.071	0.075
b	0.31	0.41	0.51	0.012	0.016	0.020
C	0.18	0.21	0.25	0.007	0.008	0.010
D	5.13	5.23	5.33	0.202	0.206	0.210
E	7.70	7.90	8.10	0.303	0.311	0.319
E1	5.18	5.28	5.38	0.204	0.208	0.212
e		1.27			0.050	
L	0.50	0.67	0.85	0.020	0.026	0.033
L1	1.21	1.31	1.41	0.048	0.052	0.056
θ	0°	5°	8°	0°	5°	8°

10.2 Package SOP8 150MIL



Symbol	mm			Inch		
	Min	Nom	Max	Min	Nom	Max
A	1.35	-	1.75	0.053	-	0.069
A1	0.10	-	0.25	0.004	-	0.010
A2	1.35	-	1.55	0.053	-	0.061
b	0.31	-	0.51	0.012	0.016	0.020
C	0.10	-	0.25	0.004	-	0.010
D	4.80	4.90	5.03	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.149	0.154	0.158
e	-	1.27	-	-	0.050	-
L	0.40	-	0.90	0.016	-	0.035
L1	0.85	1.06	1.27	0.033	0.042	0.050
θ	0°	-	8°	0°	-	8°

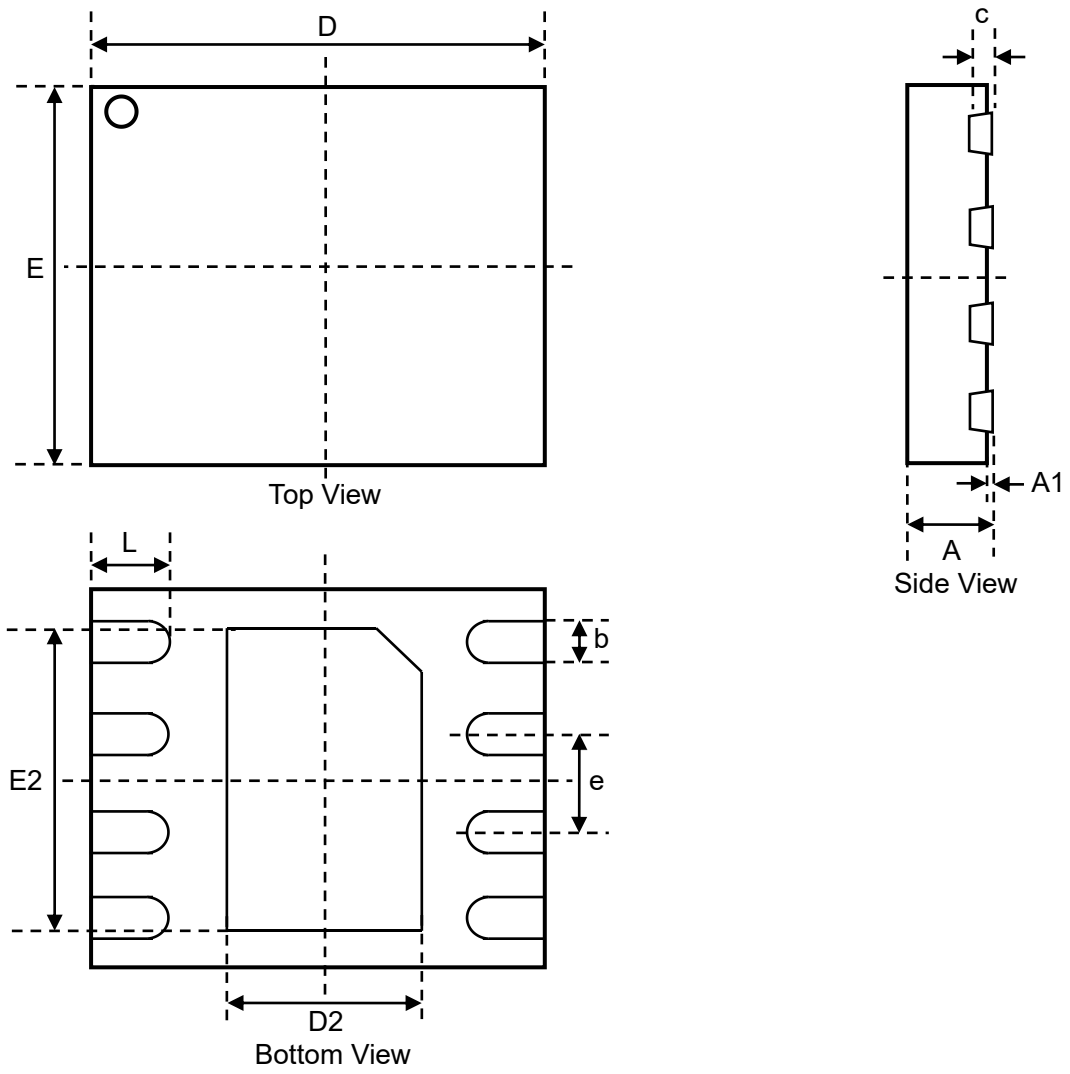
10.3 Package TSSOP8L (173mil)



Symbol	mm			Inch		
	Min	Nom	Max	Min	Nom	Max
A	-	-	1.20	-	-	0.047
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.80	0.90	1.00	0.031	0.035	0.039
b	0.20	0.25	0.30	0.008	0.010	0.012
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.90	3.00	3.10	0.114	0.118	0.112
E	6.30	6.40	6.50	0.248	0.252	0.256
E1	4.30	4.40	4.50	0.169	0.173	0.177
e	-	0.65	-	-	0.026	-
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	0.85	1.00	1.15	0.033	0.039	0.045
θ	0	4	8	0	4	8

Note:
1. The exposed metal pad area on the bottom of the package is floating.

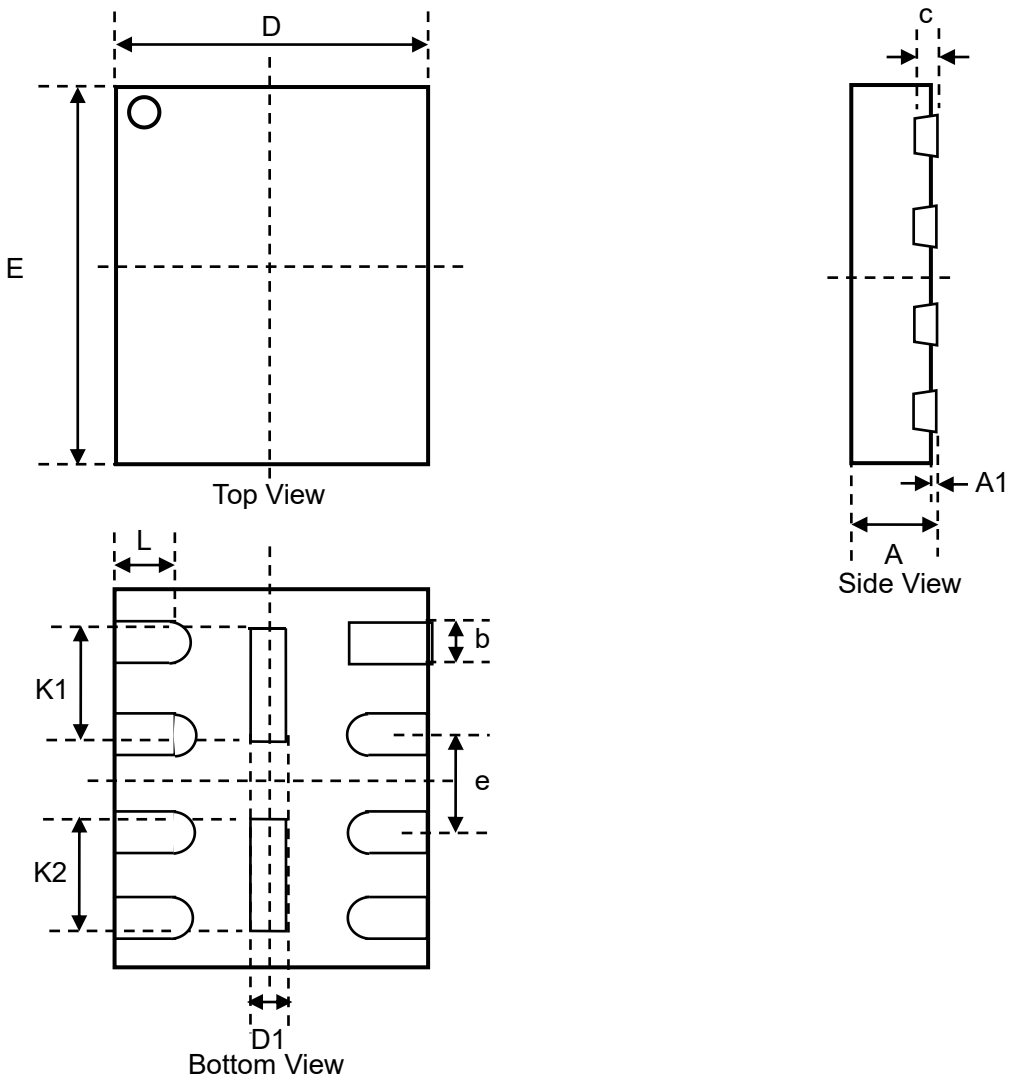
10.4 Package WSON8 (6*5mm)



Symbol	mm			Inch		
	Min	Nom	Max	Min	Nom	Max
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
c	0.18	-	0.25	0.007	-	0.010
b	0.35	0.40	0.50	0.014	0.016	0.020
D	5.90	6.00	6.10	0.232	0.236	0.240
D2	3.30	3.40	3.50	0.130	0.134	0.138
E	4.90	5.00	5.10	0.193	0.197	0.201
E2	3.90	4.00	4.10	0.154	0.157	0.161
e		1.27			0.05	
L	0.50	0.60	0.75	0.020	0.024	0.030

Note:
1.The exposed metal pad area on the bottom of the package is floating.

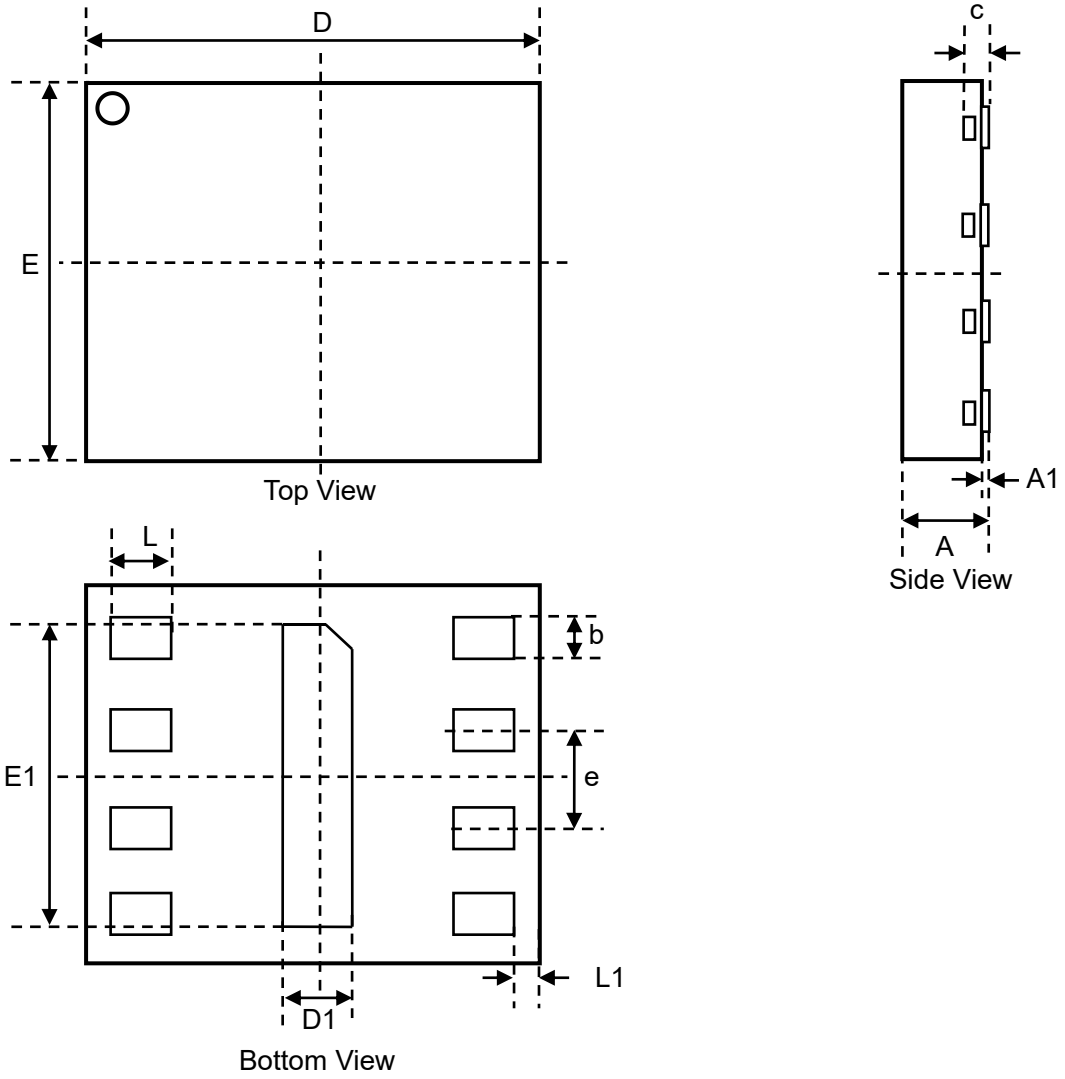
10.5 Package USON8 (4*3mm)



Symbol	mm			Inch		
	Min	Nom	Max	Min	Nom	Max
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	0.02	0.05		0.001	0.002
c	0.10	0.15	0.20	0.004	0.006	0.008
b	0.25	0.30	0.35	0.010	0.012	0.014
D	2.90	3.00	3.10	0.114	0.118	0.122
D1	0.10	0.20	0.30	0.000	0.001	0.001
E	3.90	4.00	4.10	0.154	0.157	0.161
K1	0.70	0.80	0.90	0.002	0.002	0.002
K2	0.70	0.80	0.90	0.002	0.002	0.002
e		0.80			0.031	
L	0.55	0.60	0.65	0.022	0.024	0.026

Note:
1.The exposed metal pad area on the bottom of the package is floating.

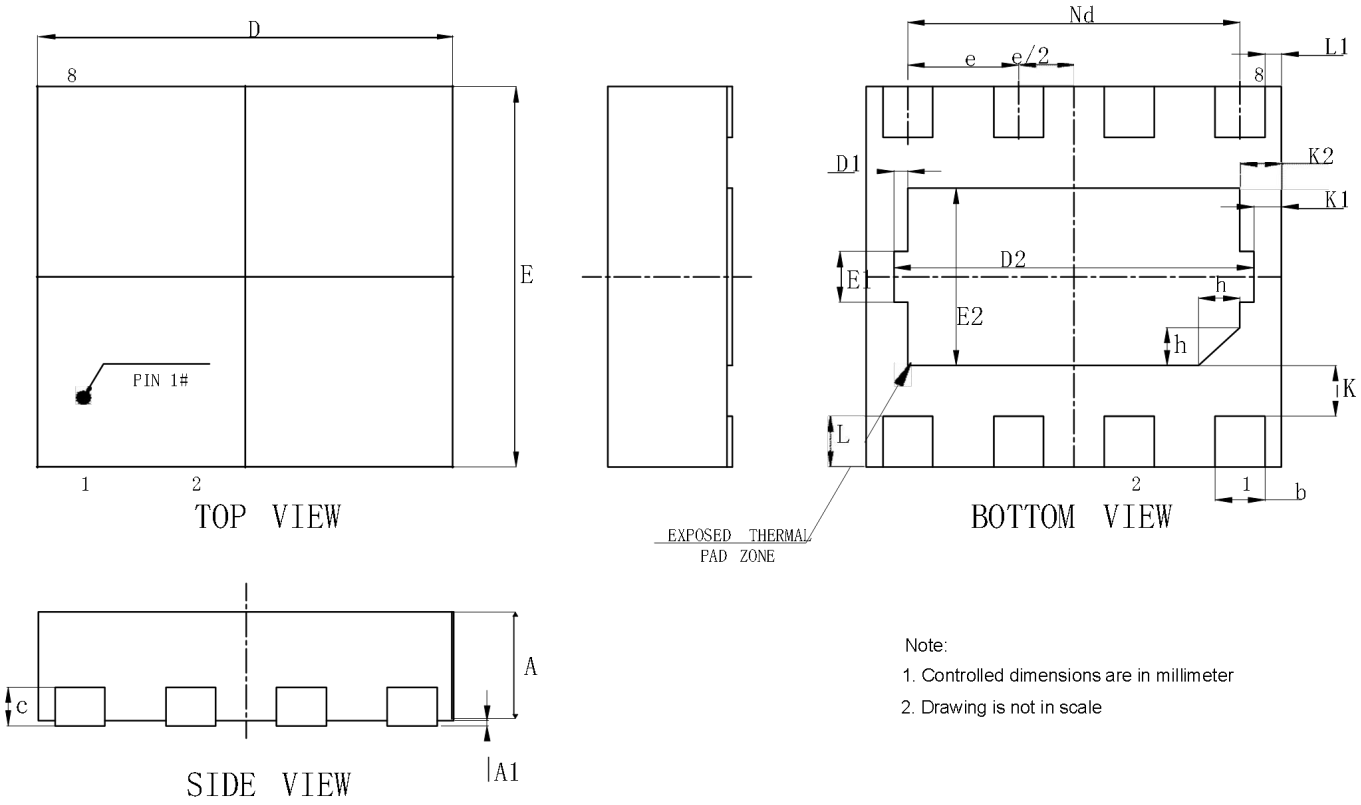
10.6 Package USON8 (2*3mm)



Symbol	mm			Inch		
	Min	Nom	Max	Min	Nom	Max
A	0.40	0.45	0.50	0.016	0.018	0.020
A1	0.00	0.02	0.05		0.001	0.002
c	0.10	-	0.20	0.004	-	0.008
b	0.20	0.25	0.30	0.008	0.010	0.012
D	2.90	3.00	3.10	0.114	0.118	0.122
D1	0.10	0.20	0.30	0.004	0.008	0.012
E	1.90	2.00	2.10	0.075	0.079	0.083
E1	1.50	1.60	1.70	0.059	0.063	0.067
e		0.50			0.020	
L	0.30	0.35	0.40	0.012	0.014	0.016
L1	0.1REF			0.004REF		

Note:
1. The exposed metal pad area on the bottom of the package is floating.

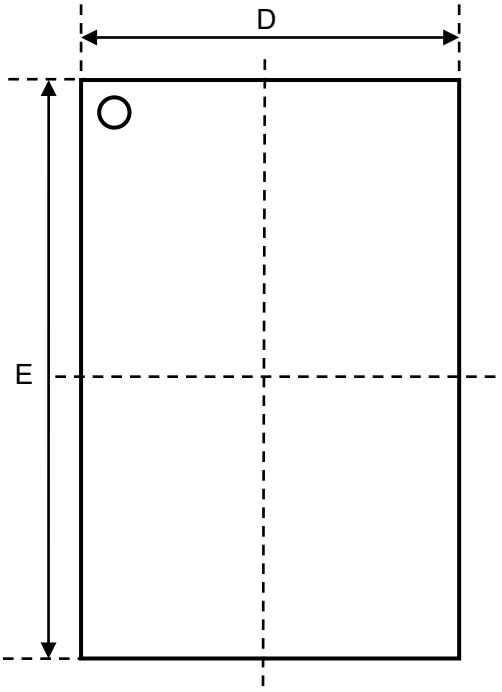
10.7 Package 8Pin USON1.5*1.5



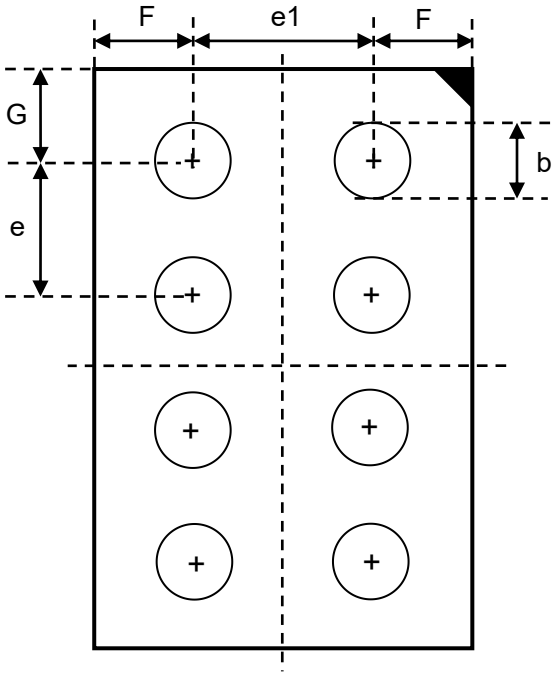
Note:
1. Controlled dimensions are in millimeter
2. Drawing is not in scale

Symbol	mm			Inch		
	Min	Nom	Max	Min	Nom	Max
A	0.400	0.450	0.500	0.016	0.018	0.020
A1	0.000	0.020	0.050	0.000	0.001	0.002
b	0.130	0.180	0.230	0.005	0.007	0.009
c		0.152		--	0.006	--
D	1.450	1.500	1.550	0.057	0.059	0.061
D1		0.050		--	0.002	--
D2	1.200	1.300	1.400	0.047	0.051	0.055
e		0.400		--	0.016	--
Nd		1.200		--	0.047	--
E	1.450	1.500	1.550	0.057	0.059	0.061
E1		0.200		--	0.008	--
E2	0.600	0.700	0.800	0.024	0.028	0.031
L	0.150	0.200	0.250	0.006	0.008	0.010
L1		0.060		--	0.002	--
K		0.200		--	0.008	--
K1		0.100		--	0.004	--
K2		0.150		--	0.006	--
h	0.100	0.150	0.200	0.004	0.006	0.008

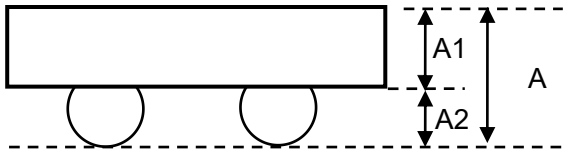
10.8 Package 8ball WLCSP



Top View



Bottom View



Side View

Symbol	mm			Inch		
	Min	Nom	Max	Min	Nom	Max
A						
A1						
A2						
b						
D						
E	-	-	-	-	-	-
F	-	-	-	-	-	-
e						
e1						
G	-	-	-	-	-	-

Note:
1. Please contact local Giantec for complete package dimensions.

11 Ordering Information

GT XXX XX X - X XX X X - XX

Company

GT=Giantec

Product Family

25Q = SPI Nor Flash,SPI/ Dual/Quad I/O

Density

05 = 512Kb	80=8Mb	128=128Mb
10 = 1Mb	16=16Mb	256=256Mb
20 = 2Mb	32=16Mb	512=512Mb
40 = 4Mb	64=16Mb	

Version

BL = BL Version

Operation Voltage

E=1.05V ~ 2.0V L = 1.65V ~ 1.95V U=1.65V ~ 3.6V H=2.7~3.6V

Package Type

W = SOP8 208 mil	VD = USON 1.5x1.5 mm
G = SOP8 150 mil	CS = WLCSP 8 ball
WS = WSON 6x5 mm	Z = TSSOP8 173mil
WU = WSON 4x3 mm	BG = BGA
ED = USON 2x3 mm	XKU30 = Sorted and Un-inked KGD

Green Code

L=Pb Free

Temperature Range

I = Industrial(-40℃ to +85℃)
IE= Industrial(-40℃ to +105℃)

Packing

TR= Tape & Reel

12 Valid Part Numbers and Top Side Marking

The following table provides the valid part numbers for the GT25Q16BL SPI Flash Memory. Please contact Giantec for specific availability by density and package type.

Density	Package Type	Product Number	Top Side Marking (-40 to 105℃)
16Mb	SOP8 208mil	GT25Q16BL-UWLI-TR	G YWW 516BLUWLI
	SOP8 150mil	GT25Q16BL-UGLI-TR	G YWW 516BLUGLI
	TSSOP 173mil	GT25Q16BL-UZLI-TR	GT 516B LUZLI YWW
	WSON 5x6	GT25Q16BL-UWSLI-TR	GT 516B LUWSU YWW
	WSON 4x3	GT25Q16BL-UWULI-TR	GT 516B LUWUU YWW
	USON 2x3	GT25Q16BL-UEDLI-TR	GT 16BL YWW
	USON 1.5x1.5	GT25Q16BL-UVDLI-TR	G6BL YWW
	WLCSP 8ball	GT25Q16BL-UCSLI-TR	

13 REVISION HISTORY

Revision	Date	Descriptions
V1.0	Feb. 2023	Initial Version
V1.1	Jul. 2025	Update AC Fr, add Top Side Marking information

Important Notice

Except for customized products which have been expressly identified in the applicable agreement, Giantec's products are designed, developed, and/or manufactured for ordinary business, industrial, personal, and/or household applications only, and not for use in any applications which may, directly or indirectly, cause death, personal injury, or severe property damages. In the event Giantec products are used in contradicted to their target usage above, the buyer shall take any and all actions to ensure said Giantec's product qualified for its actual use in accordance with the applicable laws and regulations; and Giantec as well as it’s suppliers and/or distributors shall be released from any and all liability arisen therefrom.

For the contact and order information, please visit Giantec’s Web site at: http:// www.giantec-semi.com